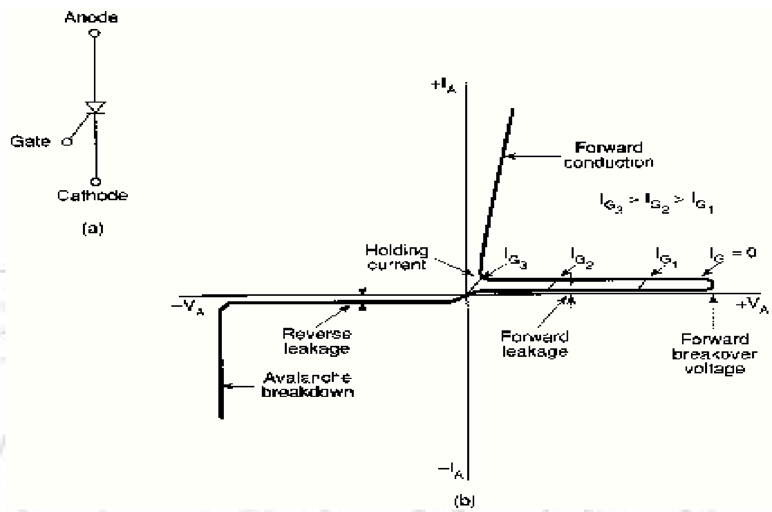
Q.No.1 a) *Draw V-I characteristics of an SCR and explain it.*

Ans: [03]



A better understanding of SCR operation can be obtained by examining the voltage-current (I-V) curve shown in Figure .This curve shows the I-V characteristics of a typical SCR. Such a curve is plotted by varying the SCR's cathode-to-anode voltage over a wide range while observing the SCR's anode current. The corresponding values are then plotted and a continuous curve is formed. The SCR is first biased in the forward direction while its gate is left open as shown in Figure 4. The SCR's cathode-to-anode voltage is designated as VF at this time. The curve shows that as VF increases from zero, the SCR conducts only a small forward current (IF) which is due to leakage. As VF continues to increase, IF remains very low and almost constant but eventually a point is reached where IF increases rapidly and VF drops to a low value (note the horizontal dotted line). The VF value required to trigger this sudden change is referred to as the Forward Break over Voltage (Vp). When this value of Vp is reached the SCR simply breaks down, and conducts a high IF which is limited only by the external resistance in series with the device. The SCR switches from the off state to the on state at this time. The drop in VF occurs because the SCR' s resistance drops to an extremely low value and most of the source voltage appears across the series resistor. When the SCR is in the on state, only a slight increase in VF is required to produce a tremendous increase in IF (the curve is almost vertical and straight). Furthermore, the SCR will remain in the on state as long as IF remains at a substantial value. Only when IF drops below a certain minimum value, will the SCR switch back to its off-state. This minimum value of IF which will hold the SCR in the on state is referred to as the SCR's Holding Current and is usually designated at IH . As shown in Figure, the IH value is located at the point where breakover occurs (just to the left of the horizontal dotted line).

When a reverse voltage is applied to the SCR as shown in Figure 4, the device functions in basically the same manner as a reverse-biased PN junction diode. As the reverse voltage

(VR) across the SCR increases from zero, only a small reverse current (IR) will flow through the device due to leakage. This current will remain small until VR becomes large enough to cause the SCR to breakdown. Then IR will increase rapidly if VR increases even slightly above the breakdown point (the curve is almost vertical and straight). The reverse voltage (VR) required to breakdown the SCR is referred to as the SCR's Reverse Breakdown Voltage. If too much reverse current is allowed to flow through the SCR after breakdown occurs, the device could be permanently damaged. However, this situation is normally avoided because the SCR is usually subjected to operating voltages which are well below its breakdown rating. [2]

b) Compare series inverter with parallel inverter.

Ans: **[1 mark /1 difference]**

Sr.no	Series inverter	Parallel inverter
1	Commutation class A	Class D
2	Resonant ckt needed	Not necessary
3	Distortion high	Low
4	Feed back not used	used
5	output wave sine	square

C) Explain function of address bus & data in 8085 microprocessor.

Ans: **Function of address bus -** **[02]**

These signals are unidirectional using that address is given by 8085 to select memory or an I/O device

Function of address bus – **[03]**

Multiplexed with address bus in operation cycle earlier part it is used as lower order address bus & in last it is used as data bus

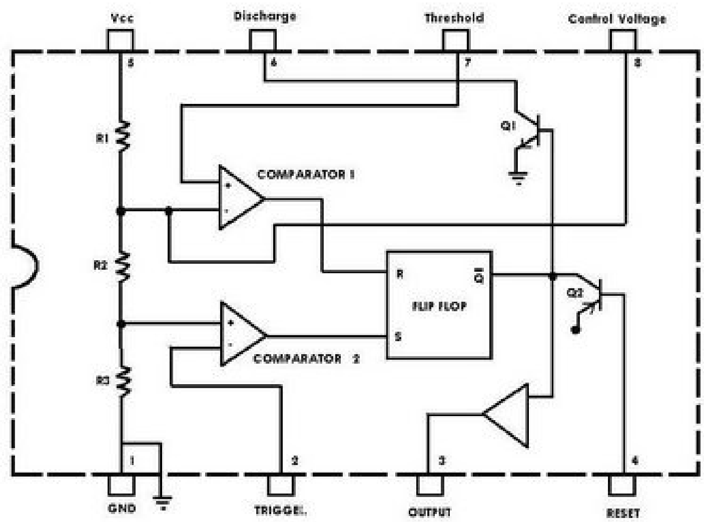
Q.No. 2.b. *With functional block diagram explain how 555 timer is used as a monostable multivibrator.*

Ans: The 555 in fig. 9a is shown here in it's utmost basic mode of operation; as a triggered monostable. One immediate observation is the extreme simplicity of this circuit. Only two components to make up a timer, a capacitor and a resistor. And for noise immunity maybe a capacitor on pin 5. Due to the internal latching mechanism of the 555, the timers will always time-out once triggered, regardless of any subsequent noise (such as bounce) on the input trigger (pin 2).

This is a great asset in interfacing the 555 with noisy sources. Just in case you don't know what 'bounce' is: bounce is a type of fast, short term noise caused by a switch, relay, etc. and then picked up by the input pin.

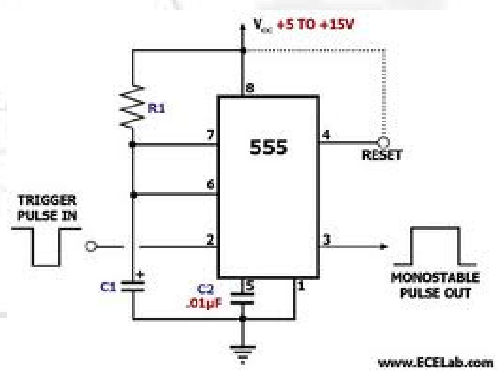
The trigger input is initially high (about 1/3 of +V). When a negative-going trigger pulse is applied to the trigger input the threshold on the lower comparator is exceeded.

The lower comparator, therefore, sets the flip-flop. That causes T1 to cut off, acting as an open circuit. The setting of the flip-flop also causes a positive-going output level which is the beginning of the output timing pulse. [2]



INTERNAL BLOCK DIAGRAM OF 555

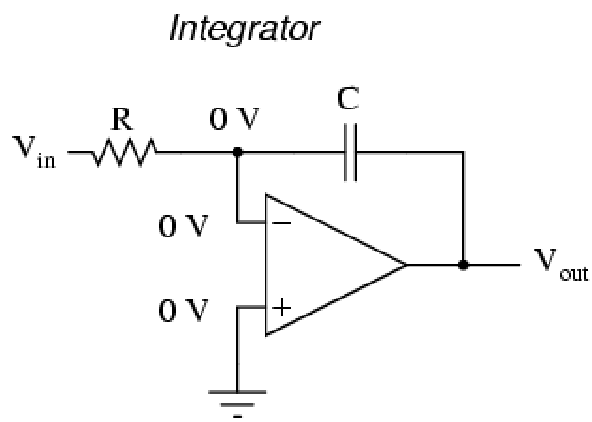
[04]



[04]

Q.No. 3.a. *Explain op-amp as integrator and derive output voltage equation*

Ans: [04]



As before, the negative feedback of the op-amp ensures that the inverting input will be held at 0 volts (the virtual ground). If the input voltage is exactly 0 volts, there will be no current through the resistor, therefore no charging of the capacitor, and therefore the output voltage will not change. We cannot guarantee what voltage will be at the output with respect to ground in this condition, but we can say that the output voltage will be constant.

However, if we apply a constant, positive voltage to the input, the op-amp output will fall negative at a linear rate, in an attempt to produce the changing voltage across the capacitor necessary to maintain the current established by the voltage difference across the resistor. Conversely, a constant, negative voltage at the input results in a linear, rising (positive) voltage at the output. The output voltage rate-of-change will be proportional to the value of the input voltage.

The formula for determining voltage output for the integrator is as follows:

$$\frac{dv_{out}}{dt} = - \frac{V_{in}}{RC}$$

or

$$V_{out} = \int_0^t - \frac{V_{in}}{RC} \, dt + c$$

Where,

c = Output voltage at start time (t=0) [4]

One application for this device would be to keep a "running total" of radiation exposure, or dosage, if the input voltage was a proportional signal supplied by an electronic radiation detector. Nuclear radiation can be just as damaging at low intensities for long periods of time as it is at high intensities for short periods of time. An integrator circuit would take both the intensity (input voltage magnitude) and time into account, generating an output voltage representing total radiation dosage.

Another application would be to integrate a signal representing water flow, producing a signal representing total quantity of water that has passed by the flowmeter. This application of an integrator is sometimes called a tantalizer in the industrial instrumentation trade [2]

Q.No. 3.b. *Explain the meaning of following instruction in case of 8085*

Ans: 1] MVI M.12H- [2 marks /instruction]

The 8-bit data is stored in the destination register or memory.

If the operand is a memory location, its location is specified by the contents of the H-L registers.

2] STA Addr:-

The contents of accumulator are copied into the memory location specified by the operand

3] JNZ Addr: - Jump if No Zero

The program sequence is transferred to the memory location specified by the 16-bit address given in the operand based on the specified flag of the PSW.

4] LHLD:-

This instruction copies the contents of memory location pointed out by 16-bit address into register L.

It copies the contents of next memory location into register H.

Example: LHLD 2040 H

5] ADD M.

The contents of register or memory are added to the contents of accumulator.

The result is stored in accumulator.

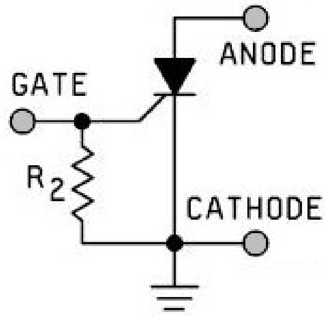
If the operand is memory location, its address is specified by H-L pair.

All flags are modified to reflect the result of the addition.

Example: ADD M

Q.No. 4.A *Explain with suitable circuit diagrams different methods of gate triggering of SCR? Under which condition SCR get mistriggered or unintentionally triggered?*

Ans: A Thyristor can be switched from a non conducting state to a conducting state in several methods: [03]



Forward voltage triggering:

In this method when anode to cathode forward voltage is increased with gate circuit open, then the reverse bias junction J2 will have a avalanche breakdown at a voltage called forward break over voltage VBO. At this voltage thyristor or SCR changes from OFF state to ON state. The forward voltage drop across the SCR during ON state is of the order of 1 to 1.5V and increases slightly with increase in the load current

Thermal Triggering (Temperature Triggering):

Width of the depletion layer of the thyristor decreases on increasing the junction temperature. Thus in the SCR when the voltage applied is very near to the breakdown voltage, the device can be triggered by increasing its junction temperature. By applying the temperature to certain extent, a situation comes when the reverse biased junction collapse making the device to conduct. This method of triggering the thyristor by heating is known as the Thermal Triggering process.

Radiation Triggering (Light Triggering):

Thyristors are bombarded with energy particles such as neutrons and protons. Light energy is focused on the depletion region results in the formation of charge carriers. This lead to instantaneous flow of current with in the device and the triggering of the device.

dv/dt Triggering:

In this method of triggering if the applied rate of change of voltage is large, then the device will turn on even though the voltage appearing across the device is small. We know that when SCR is applied with forward voltage across the anode and cathode, junctions j1 and j3 will be in forward bias and junction j2 will be in reverse bias. This reverse biased junction j2 will have the characteristics of the capacitor due to the charges exist across the junction. If the forward voltage is suddenly applied a charging current will flow tending to turn on the SCR. This magnitude of the charging current depends on the rate of change of applied voltage.

Gate Triggering:

This is the most commonly used method for triggering the SCR or thyristor. For gate triggering a signal is applied across the gate and cathode of the device. By applying a positive signal at the gate terminal of the SCR it will be triggered much before the specified break over voltage. Three types of signals can be used for triggering the SCR. They are either dc signal,ac signal or pulse signal.

DC Gate triggering:

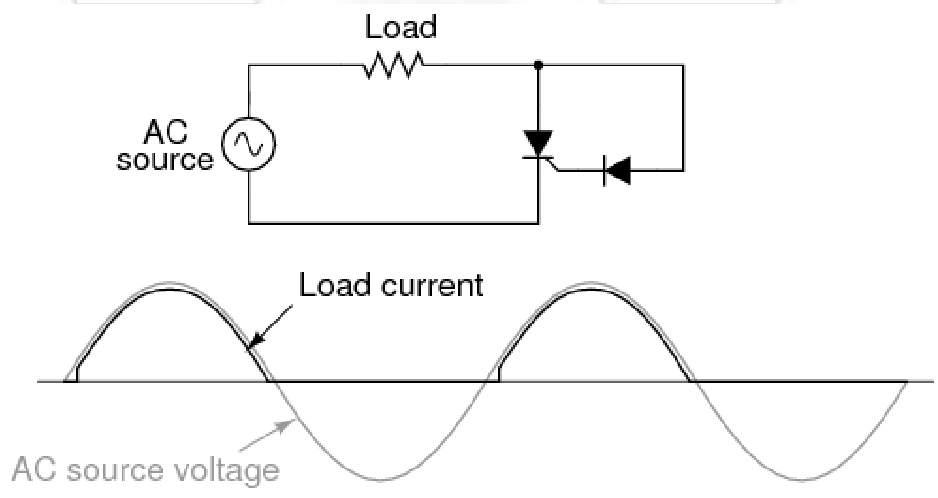
In this type of triggering a dc voltage of proper magnitude and polarity is applied between the gate and cathode such that gate becomes positive with respect to the cathode. When the applied voltage is sufficient to produce required gate current the device starts conducting

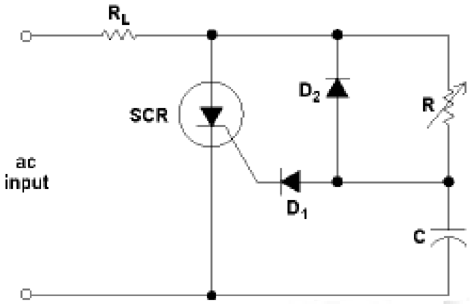
Drawbacks:

1. Both the power and control circuits are dc and there is no isolation between the two
2. continuous dc signal has to be applied to turn on the device from turning off. Hence power loss at the gate

AC Gate triggering: [03]

Ac source is most commonly used triggering source for thyristor for ac applications.





Advantages: Have the advantages than dc source such as power isolation between the power and the control circuits and firing angle can be controlled by changing the phase angle of the control signal.

Drawback:

1. Gate drive is maintained for one half cycle of the device is turned ON.
2. Severe reverse voltage is applied across gate and cathode during negative half cycle.

The drawback of this scheme is that a separate transformer is required to step down the ac supply increasing the cost

Pulse Gate Triggering: - [04]

This is the most popular method for triggering the SCR. In this method gate drive consists of single pulse appearing periodically or sequence of high frequency pulses. This is known as carrier frequency gating. A pulse transformer is used for isolation. The main advantage of this method is there is no need to apply continuous gate signal and hence gate losses are very much reduced. Electrical isolation is also provided between the main device supply and its gating signals

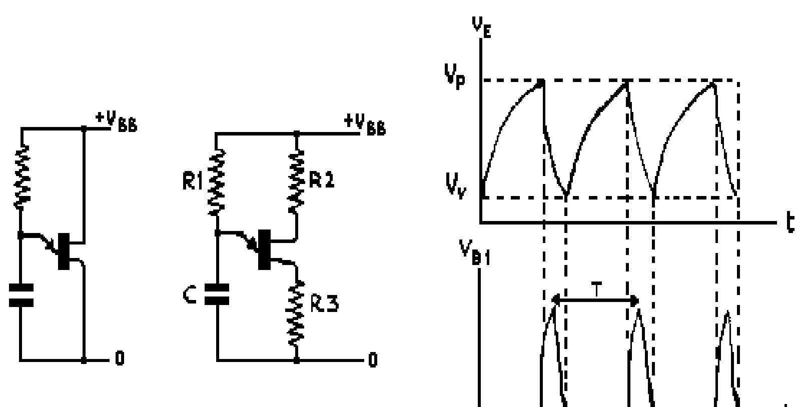


Fig.7 Fig.8 Fig.9

-- The relaxation oscillator in Figure is an application of the uni junction oscillator.

-- R1 charges C until the peak point. The unijunction emitter terminal has no effect on the capacitor until this point is reached.

-- Once the capacitor voltage, Vc, reaches the peak voltage point VP, the lowered emitter-base1 E-B1 resistance quickly discharges the capacitor.

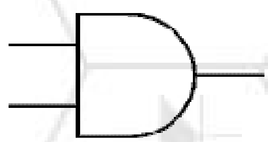
-- Once the capacitor discharges below the valley point VV, the E-RB1 resistance reverts back to high resistance, and the capacitor is free to charge again.

-- During capacitor discharge through the E-B1 saturation resistance, a pulse may be seen on the external B1 and B2 load resistors.

Q.No. 5.a *Draw the symbols truth tables and logical equations for basic gate.*

Ans: **AND gate** [2]

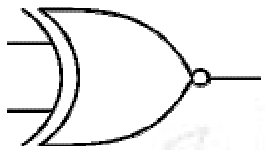
The output Q is true if input A AND input B are both true: Q = A AND B
An AND gate can have two or more inputs, its output is true if all inputs are true.



Input A	Input B	Output Q
0	0	0
0	1	0
1	0	0
1	1	1

EX-NOR (EXclusive-NOR) gate [2]

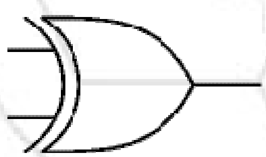
This is an EX-OR gate with the output inverted, as shown by the 'o' on the output.
The output Q is true if inputs A and B are the SAME (both true or both false):
Q = (A AND B) OR (NOT A AND NOT B)
EX-NOR gates can only have 2 inputs.



Input A	Input B	Output Q
0	0	1
0	1	0
1	0	0
1	1	1

EX-OR (Exclusive-OR) gate [2]

The output Q is true if either input A is true OR input B is true, but not when both of them are true: Q = (A AND NOT B) OR (B AND NOT A)
This is like an OR gate but excluding both inputs being true.
The output is true if inputs A and B are DIFFERENT.
EX-OR gates can only have 2 inputs.



A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

symbol

Q.No. 5.b. *Simplify Boolean equation* $Y = \bar{A}\,\bar{B}\,C + \bar{A}BC + A\bar{B}C + ABC$

Ans: $Y = \bar{A}\,\bar{B}\,C + \bar{A}BC + A\bar{B}C + ABC$

$= \bar{A}\,C\,[\bar{B} + B] + AC\,[\bar{B} + B]$

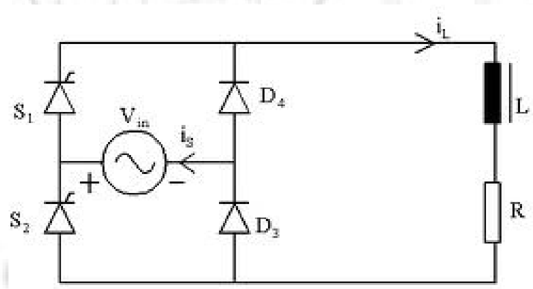
$= \bar{A}\,C + AC$ $\qquad \bar{B} + B = 1$ [02]

$= C\,[\bar{A} + A]$

$= C$ [02]

Q.No. 5.c. *Explain single phase full wave half controlled bridge rectifier.*

Ans: [04]



Configuration 2

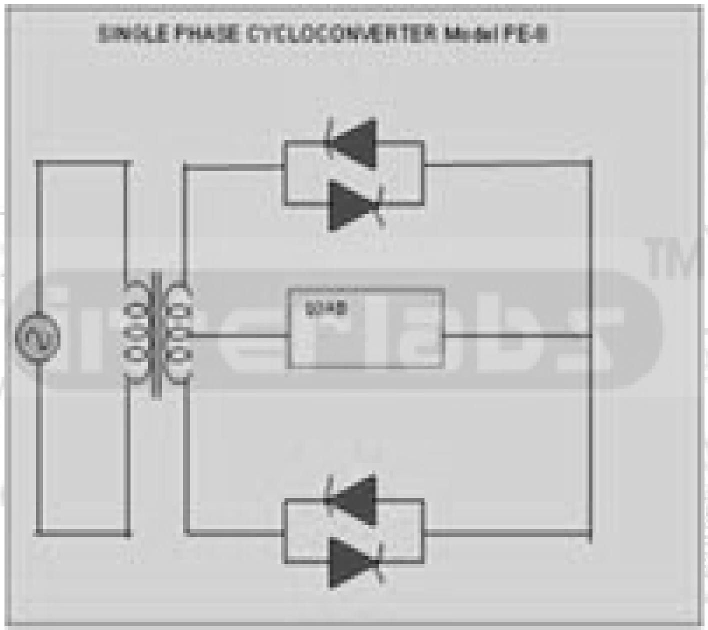
-In the positive half cycle S_1 & D_3 will conduct & gives out put across load.

-In the negative half cycle S_2 & D_2 will conduct & gives out put across load. [04]

- Wave form [02]

Q.No. 6.a *Explain single phase center tapped transformer cycloconverter. What are its Application?*

Ans: [04]



-Thyrirster s1 will conduct for first half cycle & s2 will conduct second half cycle again s1 will fired

-Depending on firing sequence we can change the frequency. [4]

-Wave form [2]

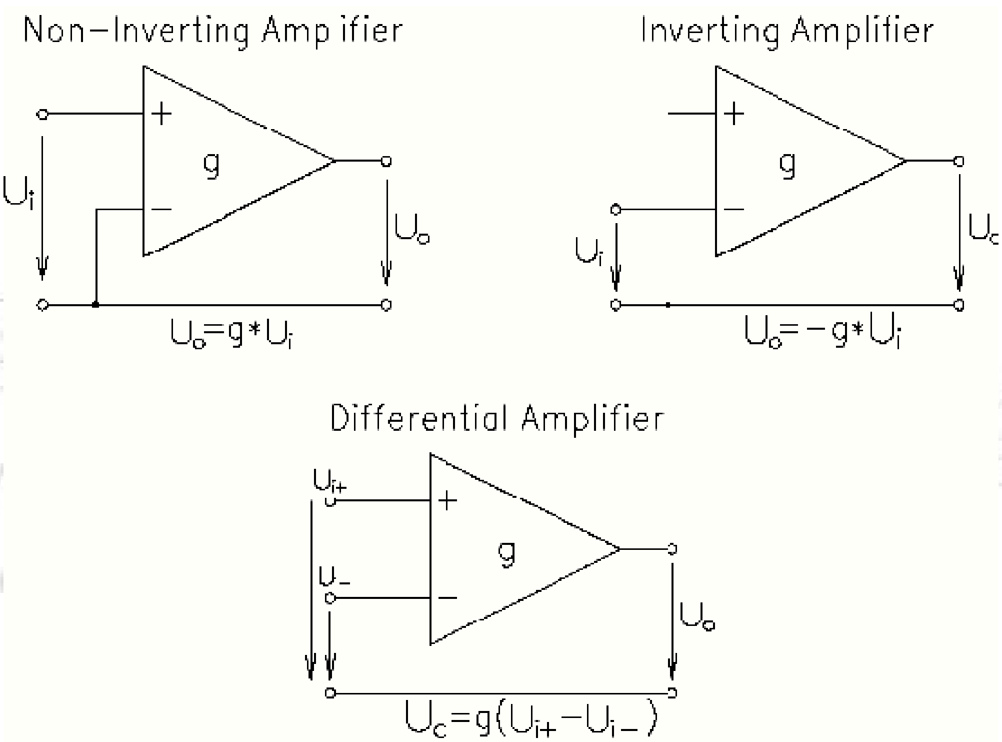
Q.No. 7.a. *Compare Natural commutation with Forced commutation of SCR.*

Ans: **[1 mark /1 difference]**

Sr.no	Natural commutation	forced commutation
1	No extra commutating component required	required
2	Power supply AC	DC
3	No power loss	Some power loss
4	No cost	costly

Q.No. 7.b. *Draw diagram of op-amp as inverting & non-inverting mode*

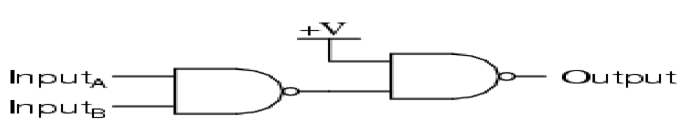
Ans: [Each 21/2]

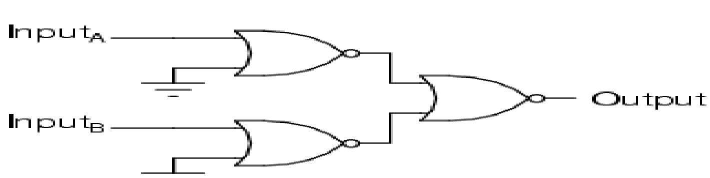


Q.No. 7.c. *Realize all basic gates using NOR gate only.*

Ans: Constructing the AND function: - [2]

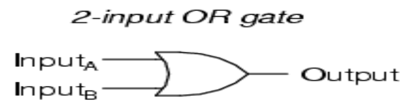
A	B	Output
0	0	0
0	1	0
1	0	0
1	1	1



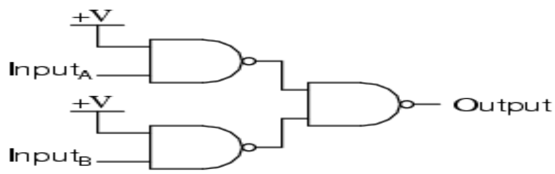


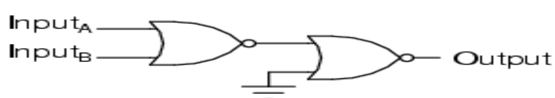
Constructing the OR functions: -

[2]



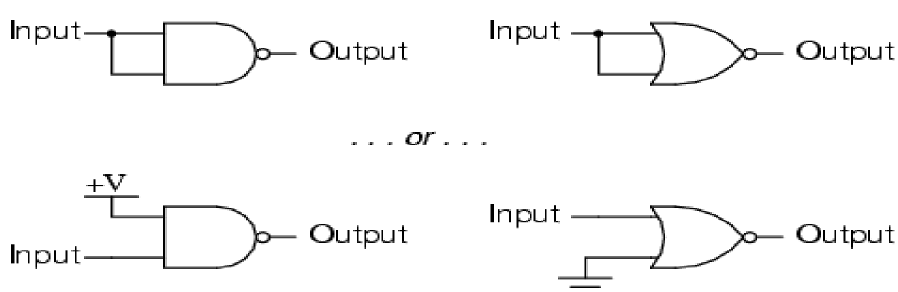
A	B	Output
0	0	0
0	1	1
1	0	1
1	1	1





Constructing the NOT function: - [1]

Input	Output
0	1
1	0



Q.No. 7.d *Explain any two addressing modes of 8085.*

Ans : Every instruction of a program has to operate on a data.

The method of specifying the data to be operated by the instruction is called Addressing. The 8085 has the following 5 different types of addressing.

1. Immediate Addressing

2. Direct Addressing

3. Register Addressing

4. Register Indirect Addressing

5. Implied Addressing

1. Immediate Addressing: [2]

In immediate addressing mode, the data is specified in the instruction itself. The data will be a part of the program instruction.

EX. MVI B, 3EH - Move the data 3EH given in the instruction to B register; LXI SP, 2700H. 2. 2. 2. Direct Addressing:

[2]

In direct addressing mode, the address of the data is specified in the instruction. The data will be in memory. In this addressing mode, the program instructions and data can be stored in different memory.

EX. LDA 1050H - Load the data available in memory location 1050H in to accumulator;

SHLD 3000H