Q.1 a) Compare BJT and FET. **(5)**

ans:

BJT	FET
1. It is a current controlled device. 2. Bipolar device. 3. Thermal runaway can damage BJT. 4. Low input impedance. 5. Noise generated by BJT is high. 6. Transfer characteristics is linear. 7. High Sensitivity. 8. Higher AC voltage gain than that of FET. 9. Bigger in size than FET. 10. Symbol.	1. It is a voltage controlled device. 2. Unipolar device. 3. Thermal runaway does not take place. 4. High input impedance. 5. Noise generated by FET is low. 6. Transfer characteristics is non-linear. 7. Low sensitivity. 8. Lesser AC voltage gain than that of BJT. 9. Smaller in size than BJT. 10. Symbol.

b) Why Common Emitter configuration is widely used in amplifier circuits. **(5)**

ans: It is the only config. that gives voltage gain and current gain greater than unity.
- CB config. has current gain less than unity and CC config. has voltage gain less than unity.
- As power gain is product of voltage gain and current gain, CE config. gives much higher power gain than CB or CC config.
- In CE ratio of o/p resistance to i/p resistance is small, may range from 10 to 100 ohms. This makes config. an ideal for coupling between various transistor stages.
- In CB or CC ratio of o/p resistance to i/p resistance is very large and hence coupling become highly inefficient due to large mismatch of resistance.

C) What do you mean by CMRR? What are the various methods to improve CMRR?

ans: CMRR is ability of differential amplifier to reject the common mode signal successfully. It is called as the figure of merit of a differential amplifier.
- CMRR is defined as the ratio of differential gain A_d and common mode gain A_c. It is defined by letter ρ.

$$CMRR = \rho = A_d / A_c$$

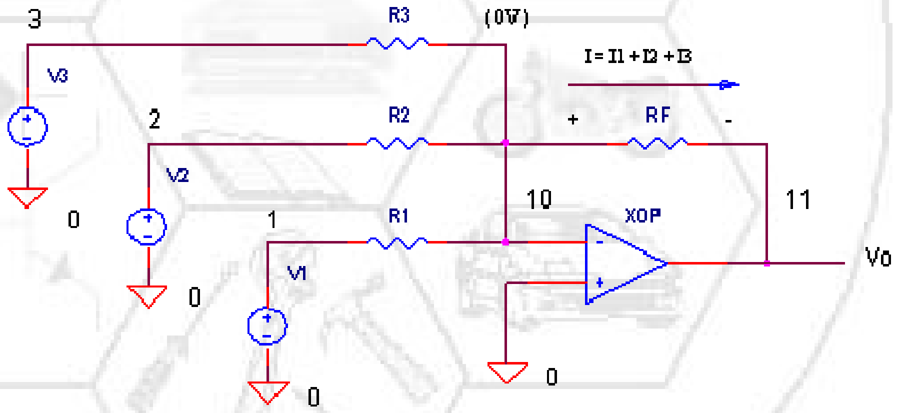
- Ideally CMRR should be infinite and practically it should be as High as possible.

METHODS TO IMPROVE CMRR:

- For improving the CMRR of the differential Amplifier using op-amp, we need to match all the resistors in the differential Amplifier to around 0.1%, becauuse 10% mismatch in resistors causes 1/5th of common mode voltage to be appeared as differential voltage, which will be amplified and appears as output noise.
- Use an instrumentation amplifier.
- Current- mode instrumentation amplifiers can be used. The method makes use of second generation current conveyors (CCII), which convert differential input voltage to equivalent current. This current is then converted back to voltage by a current to voltage converter. This configuration prevents the necessity of matching resistors for high common mode rejection. Current-mode instrumentation amplifier provides high CMRR even at low differential gains, and so can be used over a wide frequency range (note that, the gain-bandwidth product is a constant).
- The first of such method of CMRR enhancement, common- mode bootstrapping, exploits the relation between common-mode rejection and power supply rejection. In this method the CCII supply voltage is forced to follow the common-mode voltage. This method has a limitation that, it cannot be used for low voltage applications. In the second method, the output current of one CCII is subtracted from the other. The current subtraction can be done either using opamps or by inverting the current using CCII. In the third method, the performance of the CCII is improved by constructing a composite current conveyor using two or more CCII

d) **Explain summing amplifier.** **(5)**

ans: THE SUMMING AMPLIFIER



This method keeps the interaction between inputs at a minimum. That means we can change the gain or add another input without messing with the gains of the other inputs. The circuit also <u>inverts</u> the input signals.

SUMMING ACTION

Keep the potential of the negative terminal very close to the positive terminal. In this case, keep the negative terminal close to 0V (virtual ground). The op amp essentially nails one leg of R1, R2 and R3 to a 0V potential. This makes it easy to write the currents in these resistors.

I1 = V1 / R1; I2 = V2 / R2; I3 = V3 / R3

According to Kirchoff's current law, we get

I = I1 + I2 + I3

Finally, notice that one leg of RF is also kept at 0V. So the output becomes Vo = -RF x I. Combining these pieces of information, we have a simple description of the amplifier

Vo = - RF (V1 / R1 + V2 / R2 + V3 / R3)

= - (V1 · RF / R1 + V2 · RF / R2 + V3 · RF / R3)

As you can see, the gain for each input can be controlled by a single resistor.

e) **List Features of IC 555.** **(5)**

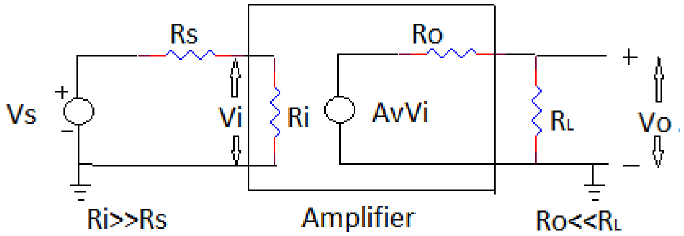
ans:

1. Can be used to provide a delay time from few microseconds through hours.
2. Operates in both Astable and Monostable mode.
3. Duty cycle of output is adjustable.
4. Sourcing and sinking capacity of output is 200mA.
5. Output and supply voltage are TTL compatible.
6. Very good temperature stability, better than 0.005% per degree Celsius.
7. Available in 8 pin MSOP package.
8. Supply voltage: single polarity 18 V maximum.
9. Power dissipation: 600 to 1100 mW.
10. Operating temperature range : 0 to 70 degree Celsius.

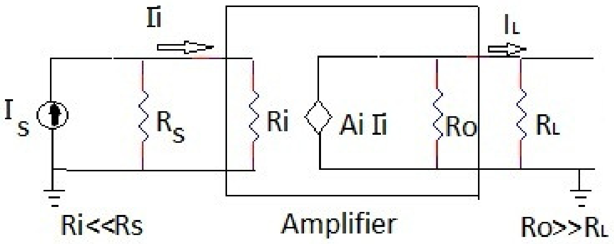
Q. 2 a) Classify and Explain feedback amplifiers. **(10)**

ans: Feedback amplifiers are classified as:

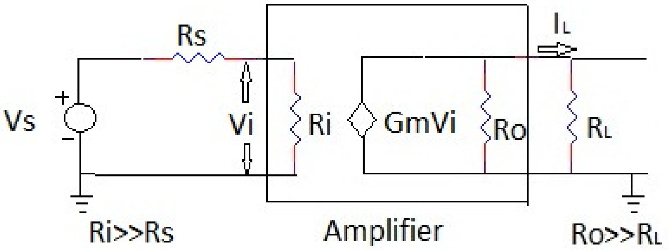
1. Voltage amplifier



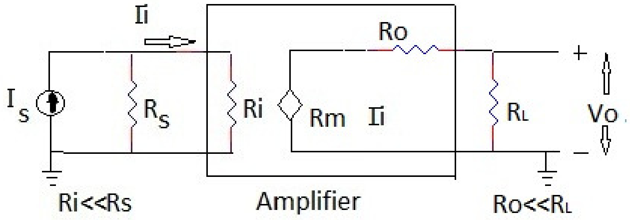
2. Current amplifier



3. Transconductance amplifier.



4. Transresistance amplifier.



Q.2 b) Explain graphical determination of h parameters using characteristic curves of CE amplifiers. (10)

ans: GRAPHICAL DETERMINATION OF THE h-PARAMETERS

Using partial derivatives (calculus), it can be shown that the magnitude of the h parameters for the small-signal transistor equivalent circuit in the region of operation for the common-emitter configuration can be found using the following equations:*

$$\boxed{h_{ie} = \frac{\partial v_i}{\partial i_i} = \frac{\partial v_{be}}{\partial i_b} \cong \frac{\Delta v_{be}}{\Delta i_b}\bigg|_{V_{CE}\,=\,\text{constant}}} \qquad \text{(ohms)}$$

$$\boxed{h_{re} = \frac{\partial v_i}{\partial v_o} = \frac{\partial v_{be}}{\partial v_{ce}} \cong \frac{\Delta v_{be}}{\Delta v_{ce}}\bigg|_{I_B\,=\,\text{constant}}} \qquad \text{(unitless)}$$

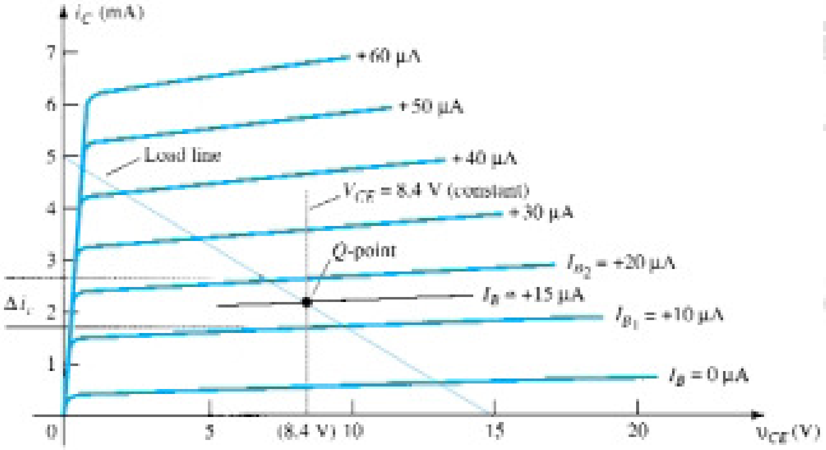
$$\boxed{h_{fe} = \frac{\partial i_o}{\partial i_i} = \frac{\partial i_c}{\partial i_b} \cong \frac{\Delta i_c}{\Delta i_b}\bigg|_{V_{CE}\,=\,\text{constant}}} \qquad \text{(unitless)}$$

$$\boxed{h_{oe} = \frac{\partial i_o}{\partial v_o} = \frac{\partial i_c}{\partial v_{ce}} \cong \frac{\Delta i_c}{\Delta v_{ce}}\bigg|_{I_B\,=\,\text{constant}}} \qquad \text{(siemens)}$$

In each case, the symbol Δ refers to a small change in that quantity around the quiescent point of operation. In other words, the h-parameters are determined in the region of operation for the applied signal so that the equivalent circuit will be the most accurate available. The constant values of V_{CE} and I_b in each case refer to a condition that must be met when the various parameters are determined from the characteristics of the transistor. For the common-base and common-collector configurations, the proper equation can be obtained by simply substituting the proper values of Vi, Vo, Ii, and Io.

The parameters hie and hre are determined from the input or base characteristics, while the parameters hfe and hoe are obtained from the output or collector characteristics.

Since hfe is usually the parameter of greatest interest, we shall discuss the operations involved with equations, for this parameter first. The first step in determining any of the four hybrid parameters is to find the quiescent point of operation as indicated in Fig. the condition VCE= constant requires that the changes in base current and collector current be taken along a vertical straight line drawn through the Q-point representing a fixed collector-to-emitter voltage. Equation then requires that a small change in collector current be divided by the corresponding change in base current. For the greatest accuracy, these changes should be made as small as possible.



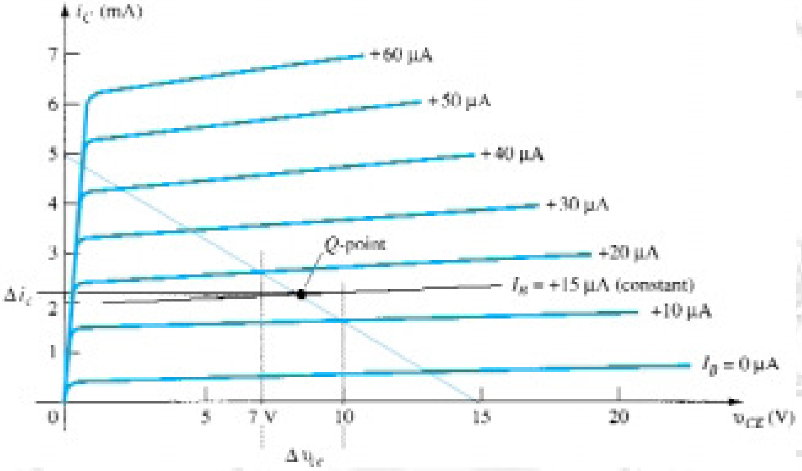
hfe determination.

In Fig. , the change in ib was chosen to extend from Ib1 to Ib2 along the perpendicular straight line at VCE. The corresponding change in ic is then found by drawing the horizontal lines from the intersections of IB1 and IB2 with VCE=constant to the vertical axis. All that remains is to substitute the resultant changes of Ib and Ic into Eq. That is,

$$|h_{fe}| = \frac{\Delta i_c}{\Delta i_b}\bigg|_{V_{CE}\,=\,\text{constant}} = \frac{(2.7 - 1.7)\ \text{mA}}{(20 - 10)\ \mu\text{A}}\bigg|_{V_{CE}\,=\,8.4\ \text{V}}$$

$$= \frac{10^{-3}}{10 \times 10^{-6}} = \mathbf{100}$$

In Fig., a straight line is drawn tangent to the curve *IB* through the *Q*-point to establish a line *IB*=constant as required by Eq. for *hoe*. A change in *Vce* was then chosen and the corresponding change in Ic determined by drawing the horizontal lines to the vertical axis at the intersections on the *IB*= constant line. Substituting into Eq. we get



hoe determination

$$|h_{oe}| = \frac{\Delta i_c}{\Delta v_{ce}}\bigg|_{I_B\,=\,\text{constant}} = \frac{(2.2 - 2.1)\ \text{mA}}{(10 - 7)\ \text{V}}\bigg|_{I_B\,=\,+15\ \mu\text{A}}$$

$$= \frac{0.1 \times 10^{-3}}{3} = \mathbf{33\ \mu A/V = 33 \times 10^{-6}\ S = 33\ \mu S}$$

.

$$|h_{ie}| = \left.\frac{\Delta v_{be}}{\Delta i_b}\right|_{V_{CE}\,=\,\text{constant}} = \left.\frac{(733 - 718)\ \text{mV}}{(20 - 10)\ \mu\text{A}}\right|_{V_{CE}\,=\,8.4\ \text{V}}$$

$$= \frac{15 \times 10^{-3}}{10 \times 10^{-6}} = \mathbf{1.5\ k\Omega}$$

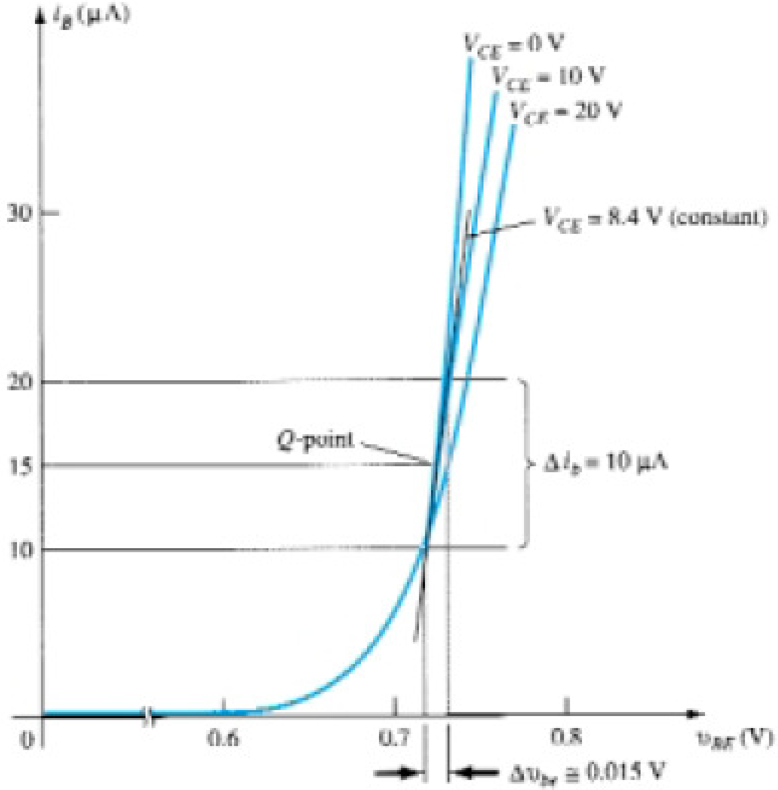
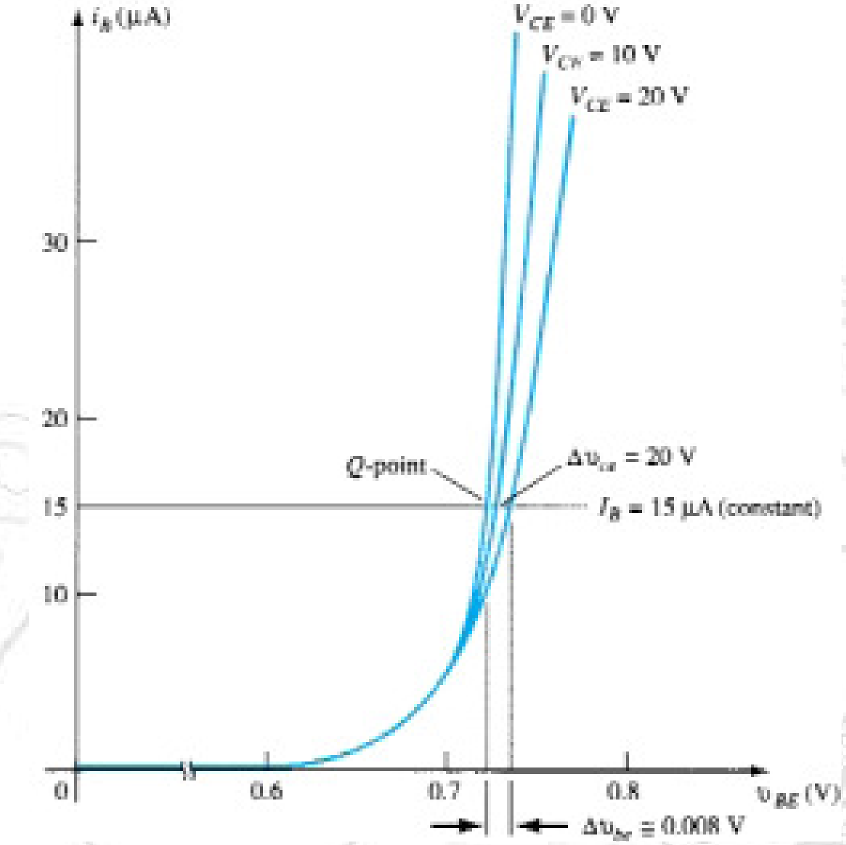


Figure 7.42 h_{ie} determination.

The last parameter, *hre*, can be found by first drawing a horizontal line through the *Q*-point at *IB*=15 µA. The natural choice then is to pick a change in Vce and find the resulting change in V*be* as shown in Fig., Substituting into Eq., we get

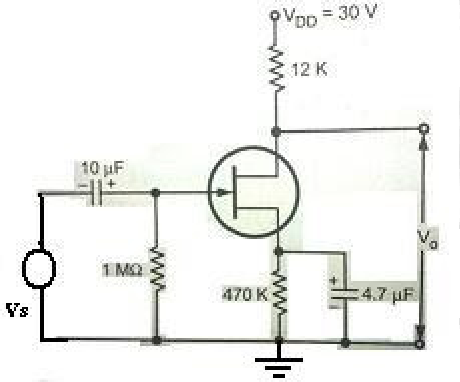
$$|h_{re}| = \left.\frac{\Delta v_{be}}{\Delta v_{ce}}\right|_{I_B\,=\,\text{constant}} = \frac{(733 - 725)\ \text{mV}}{(20 - 0)\ \text{V}} = \frac{8 \times 10^{-3}}{20} = \mathbf{4 \times 10^{-4}}$$



hre determination

As mentioned earlier, the hybrid parameters for the common-base and common collector configurations can be found using the same basic equations with the proper variables and characteristics.

Q. 3 a) FET amplifier shown below has following parameters
Idss= 3 mA, Vp= -4 V, rd >> Rd
Determine V_{GS}, I_D, V_{DS}, and Av **(10)**



Gm= Gmo= 2Idss/Vp= 1.5mS

ans: $Id= Idss(1-Vgs/Vp)^2$

$Vgs= -IdRs$

Solving for Id we get Id= 9.015μA or 8.038μA

Vgs for Id= 9.015 Vgs= -4.24V

But Vgs can't be greater than Vp

Hence

Id=8.038μA

Vgsq= -3.78V

Appying KVL to output circuit we have,

30-Id(Rs+Rd)-Vdsq= 0

Vdsq= 26.126V

Voltage Gain Av= -Gm(Rd||rd)=-GmRd since rd>>Rd

Av= -0.99

Q. 3 b) **Explain construction and working of n-channel JFET with help of characteristic curves**. **(10)**

ans: The JFET is a three-terminal device with one terminal capable of controlling the current between the other two.The basic construction of the n-channel JFET is shown in Fig. The major part of the structure is the n-type material that forms the channel between the embedded layers of p-type material. The top of the n-type channel is connected through an ohmic contact to a terminal referred to as the drain (D), while the lower end of the same material is connected through an ohmic contact to a terminal referred to as the source (S). The two p-type materials are connected together and to the gate (G) terminal. In essence, therefore, the drain and source are connected to the ends of the n-type channel and the gate to the two layers of p-type material. In the absence of any applied potentials the JFET has two p-n junctions under no-bias conditions. The result is a depletion region at each junction as shown in Fig.that resembles the same region of a diode under no-bias conditions. Depletion region is that region void of free carriers and therefore unable to support conduction through the region.

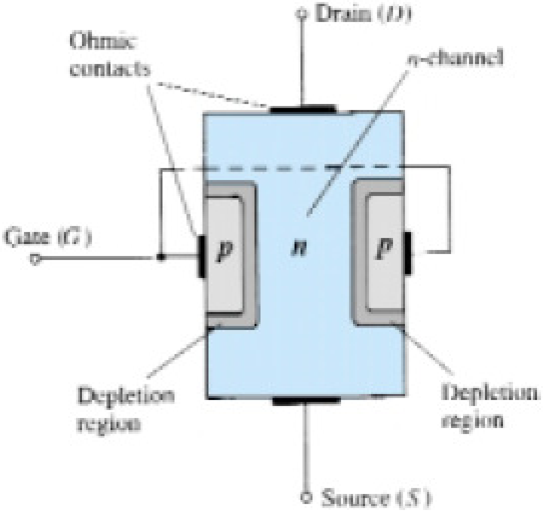


Figure 5.2 Junction field-effect transistor (JFET).

VGS =0 V, VDS= Some Positive Value

In Fig., a positive voltage VDS has been applied across the channel and the gate has been connected directly to the source to establish the condition VGS =0 V. The result is a gate and source terminal at the same potential and a depletion region in the low end of each p-material similar to the distribution of the no-bias conditions. The instant the voltage VDD (> VDS) is applied, the electrons will be drawn to the drain terminal, establishing the conventional current ID with the defined direction of Fig. The path of charge flow clearly reveals that the drain and source currents are equivalent (ID = IS). Under the conditions appearing in Fig., the flow of charge is relatively uninhibited and limited solely by the resistance of the n-channel between drain and source.

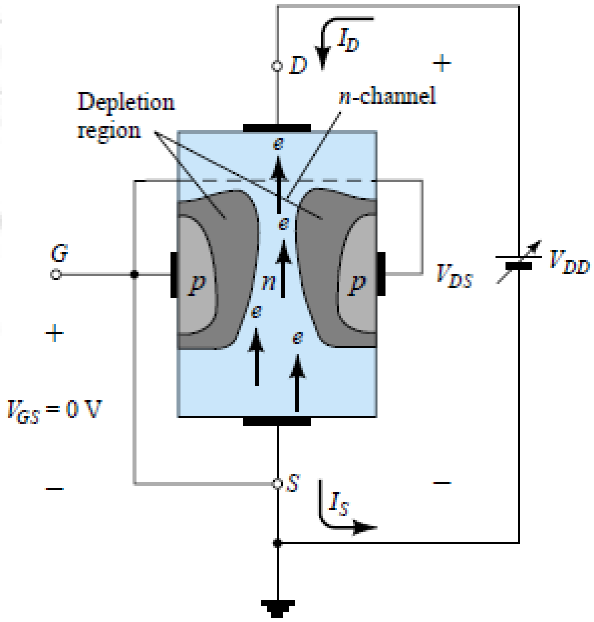


Figure 5.4 JFET in the $V_{GS} = 0$ V and $V_{DS} > 0$ V.

As the voltage VDS is increased from 0 to a few volts, the current will increase as determined by Ohm’s law and the plot of ID versus VDS will appear as shown in Fig. The relative straightness of the plot reveals that for the region of low values of VDS, the resistance is essentially constant. As VDS increases and approaches a level referred to as VP in Fig., the depletion regions will widen, causing a noticeable reduction in the channel width. The reduced path of conduction causes the resistance to increase and the curve in the graph to occur. The more horizontal the curve, the higher the resistance, suggesting that the resistance is approaching “infinite” ohms in the horizontal region. If VDS is increased to a level where it appears that the two depletion regions would “touch” as shown in Fig., a condition referred to as pinch-off will result. The level of VDS that establishes this condition is referred to as the pinch-off voltage and is denoted by VP . In actuality, the term pinch-off is a misnomer in that it suggests the current ID is pinched off and drops to 0 A. however, this is hardly the case— ID maintains a saturation level defined as IDSS in Fig. In reality a very small channel still exists, with a current of very high density. The fact that ID does not drop off at pinch-off and maintains the saturation level indicated in Fig.is verified by the following fact: The absence of a drain current would remove the possibility of different potential levels through the n-channel material to establish the varying levels of reverse bias along the p-n junction. The result would be a loss of the depletion region distribution that caused pinch-off in the first place.

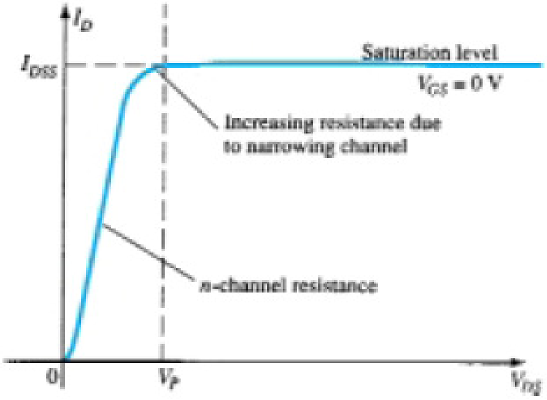


Figure 5.6 I_D versus V_{DS} for $V_{GS} = 0$ V.

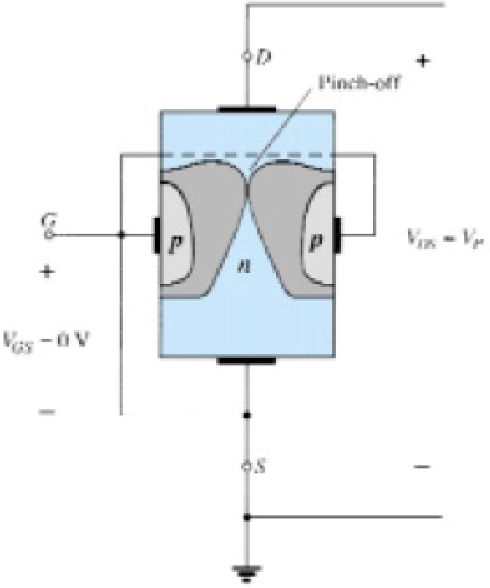


Figure 5.7 Pinch-off ($V_{GS} = 0$ V, $V_{DS} = V_P$).

As VDS is increased beyond VP, the region of close encounter between the two depletion regions will increase in length along the channel, but the level of ID remains essentially the same. In essence, therefore, once VDS = VP the JFET has the characteristics of a current source. As shown in Fig., the current is fixed at ID = IDSS, but the voltage VDS (for levels < VP) is determined by the applied load. The choice of notation IDSS is derived from the fact that it is the Drain-to-Source current with a Short-circuit connection from gate to source. As we continue to investigate the characteristics of the device we will find that:

IDSS is the maximum drain current for a JFET and is defined by the conditions VGS =0 V and VDS= |VP|.

Note that VGS =0 V for the entire length of the curve. The next few paragraphs will describe how the characteristics of Fig.are affected by changes in the level of VGS.

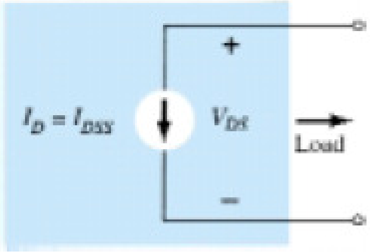


Figure 5.8 Current source equivalent for $V_{GS} = 0$ V, $V_{DS} > V_P$.

VGS <0 V

The voltage from gate to source, denoted VGS, is the controlling voltage of the JFET. Just as various curves for IC versus VCE were established for different levels of IB for the BJT transistor, curves of ID versus VDS for various levels of VGS can be developed for the JFET. For the n-channel device the controlling voltage VGS is made more and more negative from its VGS = 0 V level. In other words, the gate terminal will be set at lower and lower potential levels as compared to the source. In Fig. a negative voltage of -1 V has been applied between the gate and source terminals for a low level of VDS. The effect of the applied negative-bias VGS is to establish depletion regions similar to those obtained with VGS =0 V but at lower levels of VDS. Therefore, the result of applying a negative bias to the gate is to reach the saturation level at a lower level of VDS as shown in Fig. for VGS=-1 V. The resulting saturation level for ID has been reduced and in fact will continue to decrease as VGS is made more and more negative. Note also on Fig how the pinchoff voltage continues to drop in a parabolic manner as VGS becomes more and more negative. Eventually, VGS when VGS=-VP will be sufficiently negative to establish a saturation level that is essentially 0 mA, and for all practical purposes the device has been “turned off.” In summary:

The level of VGS that results in ID =0 mA is defined by VGS = VP, with VP being a negative voltage for n-channel devices and a positive voltage for p-channel JFETs.

On most specification sheets the pinch-off voltage is specified as VGS(off) rather than VP. A specification sheet will be reviewed later in the chapter when the primary elements of concern have been introduced. The region to the right of the pinch-off locus of Fig. is the region typically employed in linear amplifiers (amplifiers with minimum distortion of the applied signal) and is commonly referred to as the constant-current, saturation, or linear amplification region.

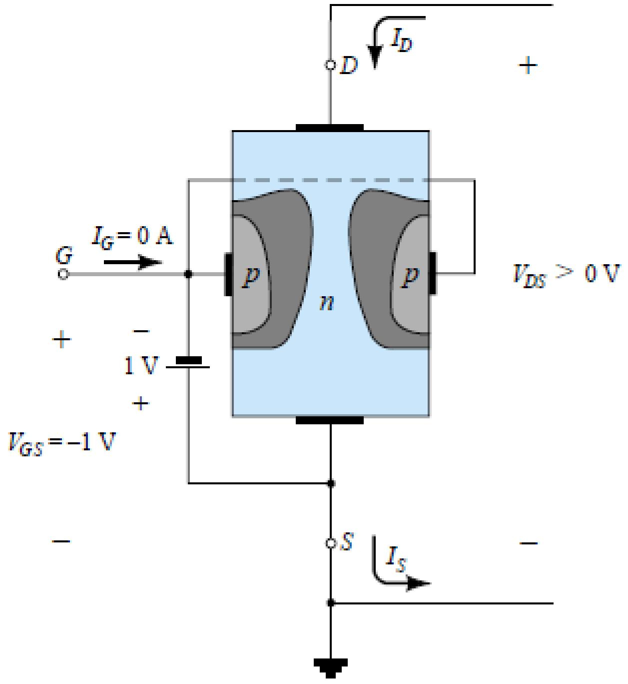


Figure 5.9 Application of a negative voltage to the gate of a JFET.

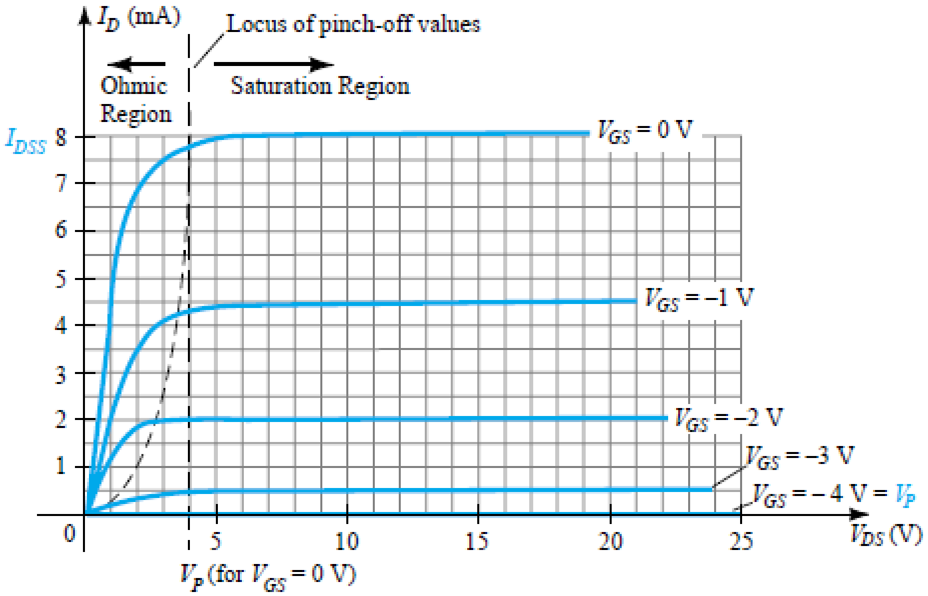
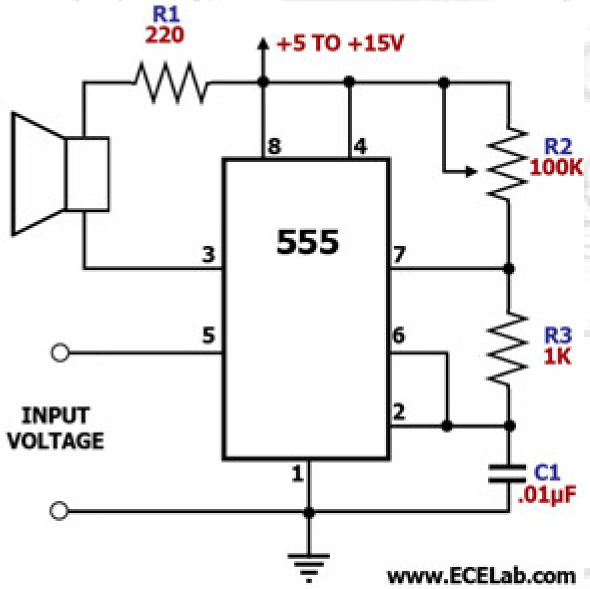


Figure 5.10 *n*-Channel JFET characteristics with $I_{DSS} = 8$ mA and $V_P = -4$ V.

Q. 4 a) **Explain any 2 applications of Astable Multivibrator using IC 555.** **(10)**

ans: Application 1: Voltage Controlled Oscillator

555 Timer Voltage-Controlled Oscillator



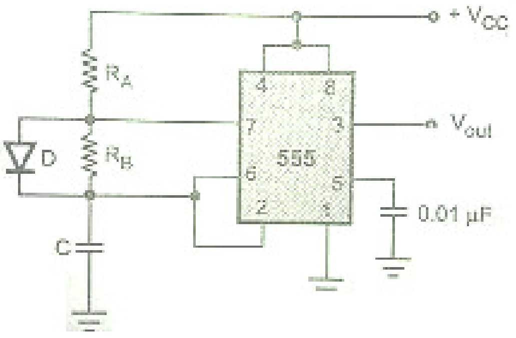
555 Timer Voltage-Controlled Oscillator Circuit Diagram

This circuit is a voltage-controlled oscillator (VCO) that uses the 555 timer IC as the main component. As expected, the 555 timer is configured as an astable multivibrator to be able to serve as an oscillator. An astable multivibrator is just a timing circuit whose output oscillates between 'low' and 'high' continuously, in effect generating a train of pulses.

The difference of this circuit with the basic 555 astable circuit is that its 555's pin 5 is tied to an external voltage source. Pin 5 is the 555's control voltage pin, which allows the user to directly adjust the threshold voltages to which the pin 2/pin 6 input voltages are compared by the 555's internal comparators. Since the outputs of these comparators control the internal flip-flop that toggles the output of the 555, adjusting the pin 5 control voltage also adjusts the frequency at which the 555 toggles its output. Increasing the input voltage at pin 5 decreases the output oscillation frequency while decreasing the input voltage increases the output oscillation frequency.

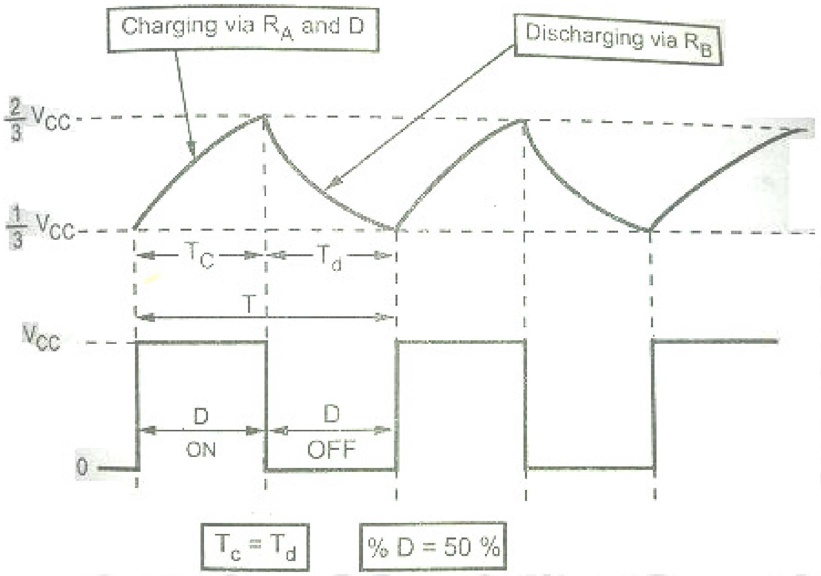
Application 2: Square Wave Generator

Circuit Diagram:



- In astable multivibrator exact 50% duty cycle is not achievable. To obtain square wave of exact 50% duty cycle, a diode D is connected in parallel to resistance Rb as shown in figure.
- Here capacitor C charges through Ra and diode D and discharges through Rb.
- To obtain square wave Rb is adjusted such that it is equal to summation of resistance Ra and forward resistance of diode D. Usually potentiometer is used for exact adjustments of resistors.

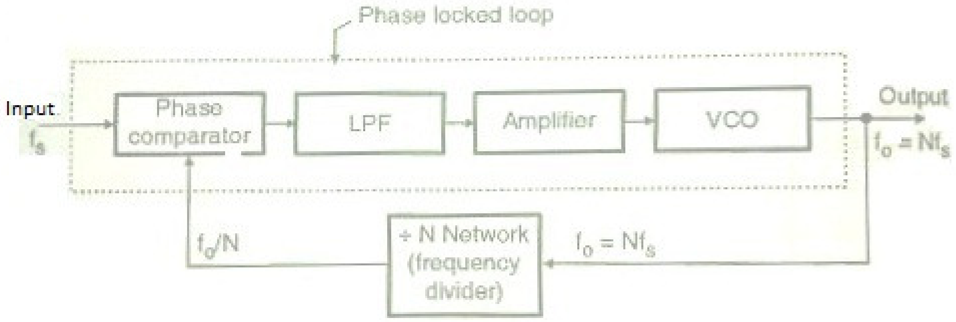
Waveforms:



b) **Explain any 2 applications of IC 565 PLL.** **(10)**

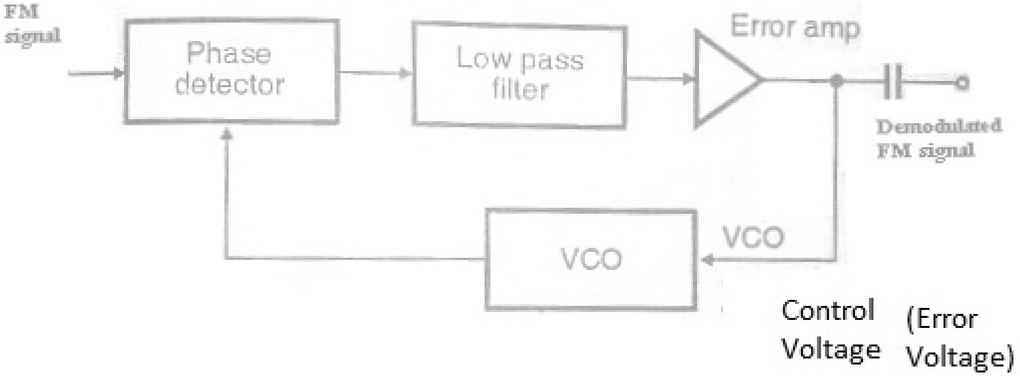
ans: Application 1: Frequency Multiplication/Division

Block Diagram:



- A divide by N network is connected externally between VCO output and phase comparator input.
- Since output of divider network is locked to the input frequency fs, the VCO actually operates at a frequency which is N times higher than fs.
- Hence fo=Nfs
- Multiplying factor can be obtained by proper selection of scaling factor N of the frequency divider.

Application 2: FM detection using PLL

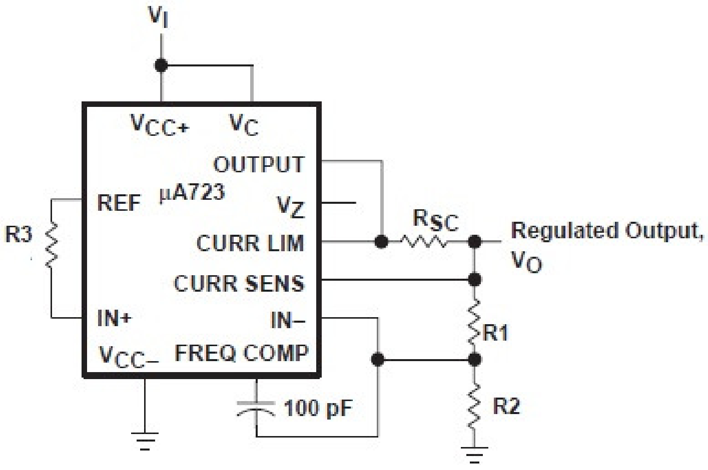


Block Diagram:

- The FM signal which is to be demodulated is applied at the input of the PLL.
- As the PLL is locked to FM signal, the VCO starts tracking instantaneous frequency in the FM input signal.
- Error voltage produced at the output of amplifier is proportional to the deviation of input frequency from the center frequency of FM. Thus the AC component of the error voltage represents the modulating signal. Thus at the error amplifier output we get demodulated FM output.

Q. 5 a) **Explain a High Voltage Low current regulator and low voltage high current regulator.** **(10)**

ans: High Voltage Low current regulator



A. R3 = $\frac{R1 \times R2}{R1 + R2}$ for a minimum α_{V_O}

B. R3 can be eliminated for minimum component count. Use direct connection (i.e., $R_3 = 0$).

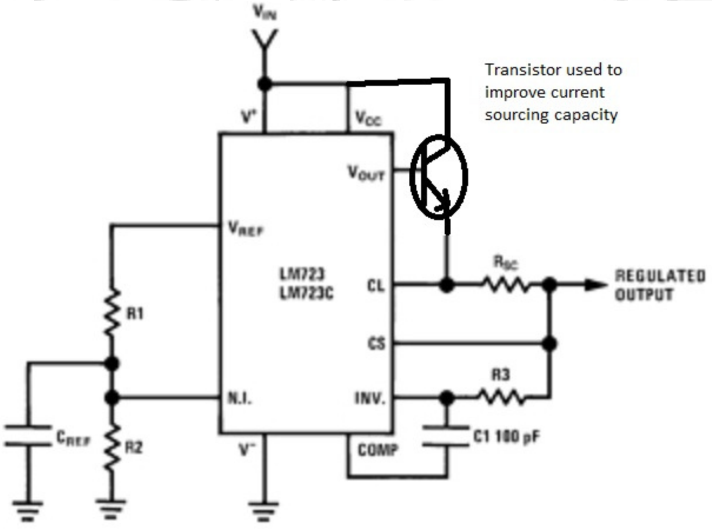
Basic High voltage low current regulator $(V_O = 7\ V\ to\ 37\ V)$

Voltage range between 7V to 37V

Maximum load current of 150 mA

Vo= (1+R1/R2). Vref
Rsc= 0.6/I $_{\text{limit}}$
R3= R1 ll R2

Low voltage high current regulator.



Transistor used to improve current sourcing capacity

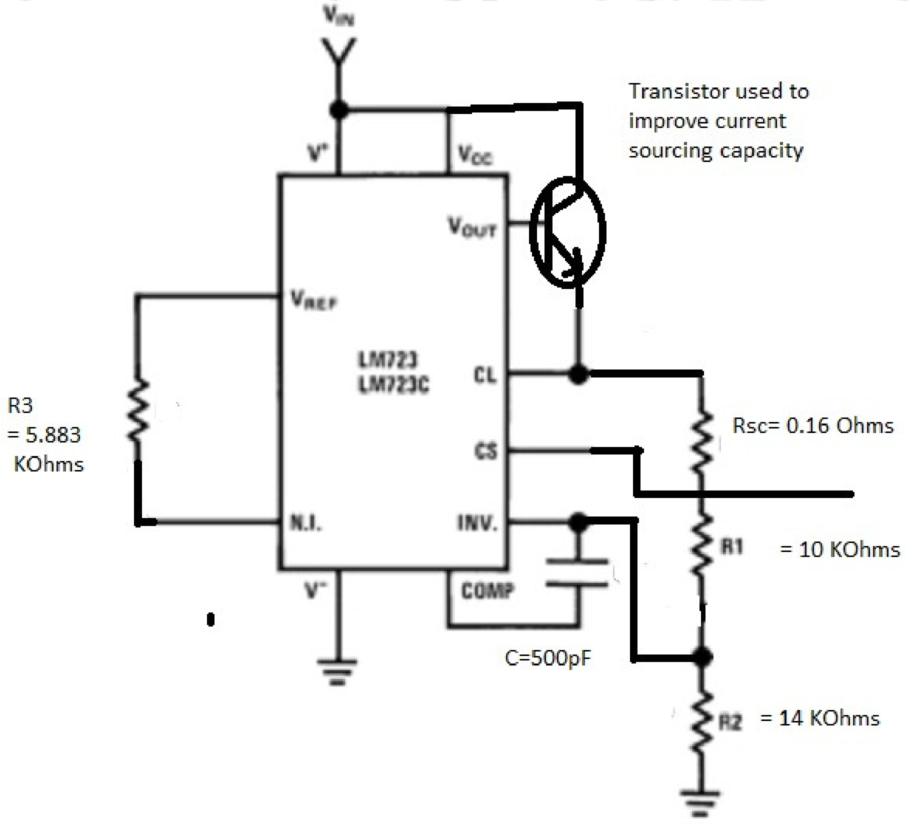
- Voltage range 2V to 7V
- Vo= R2/(R1+R2). Vref

- Rsc= 0.6/I_{limit}
- R1= (Vref- Vo)/I
- R2= Vo/I
- R3= R1||R2

Transistor is used to improve current sourcing capacity.

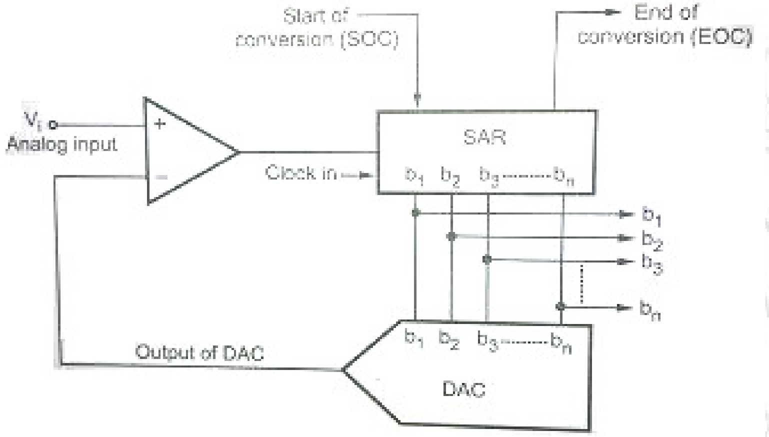
B) **Design a regulator using LM 723 for Vo=9V and Io=3A.** **(10)**

ans: I_{limit}= 1.2 Io= 3.6A
Rsc= 0.6/ I_{limit}= 0.16 ohms
Vref= 7 V for IC723
Vo= Vref(R1+R2)/R2
9= 7(R1+R2)/R2
2R2= 7R1
Choose R1=10KOhms hence R2= 14KOhms
R3= R1|| R2
R3= 5.883 KOhms



Q.6 a) **Draw and Explain Successive approximation register type ADC.** **(10)**
ans:

1. This technique uses an efficient ‘code search’ strategy to complete the n-bit conversion in just n clock periods.
2. Thus it takes much shorter conversion time as compared to counter type ADC.
3. CIRCUIT DIAGRAM:



4. Operation:

a. SAR receives the comparator output, clock and start of conversion signals and produces n-bit digital output along with end of conversion signal.
b. If Vd < Va then comparator o/p goes high which is applied to SAR.
c. If initial bits are b2b1b0=100 (3-bit ADC) then for high comparator o/p, SAR keeps b2=1 and makes b1=1 otherwise(for low comparator o/p) it resets b2=0 and makes b1=1. The same process is repeated for b1 and b0.
d. The status of b0, b1 and b2 gives digital equivalent of analog input.

Advantages:

a. Conversion time = n clock period for n-bit ADC.
b. Conversion time is constant and independent of Va.

Disadvantages:

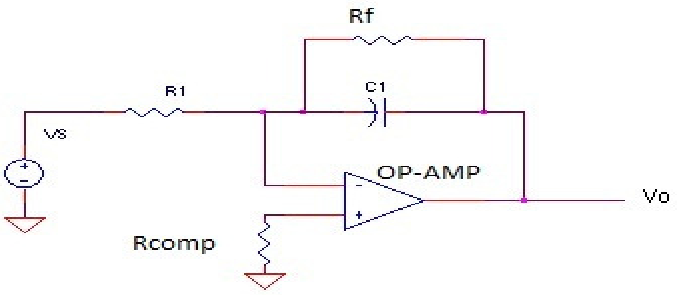
a. Complex circuit.
b. Conversion time is more compared to flash type ADC.

Applications:

Most widely used in Microprocssor based data acquisition systems.

b) Explain working of practical integrator. Also explain its advantages over a simple integrator. (10)

ans: Circuit Diagram:



Analysis:

- As input current of op-amp is zero, node B is at ground potential.
- Hence node A is also at ground potential from the concept of virtual ground. So Va= 0.
- From fig.

I= Vin-Va/R1= Vin/R1

Similarly

I1= Cf d(Va-Vo)/dt= -Cf dVo/dt

And

I2= -Vo/Rf

At node A, applying KCL

I= I1 + I2

Vin/R1= -Cf dVo/dt – Vo/Rf

Taking Laplace transform and solving it we get,

Vo(s)= - 1/sR1Cf . Vin(s)

Taking inverse Laplace Transform

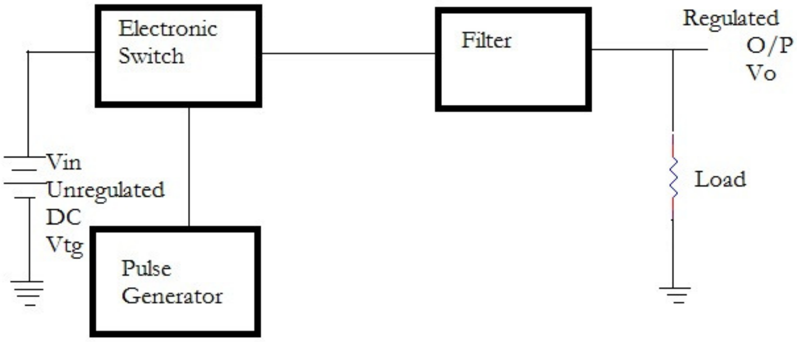
Vo(t)=-1/R1Cf . ∫ Vin (t) dt

Advantages over simple Integrator:

1. The resistance R_{comp} is used to overcome errors due to the bias current.
2. The resistance Rf reduces the low frequency gain of the op-amp.
3. Due to presence of Rf bandwidth of practical integrator is much larger than ideal integrator.

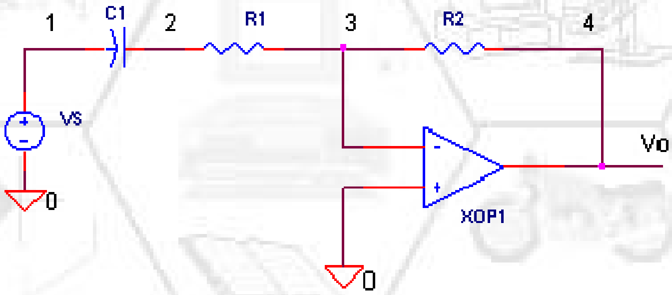
Q. 7 Write short notes on:

A) Switching Regulator **(5)**



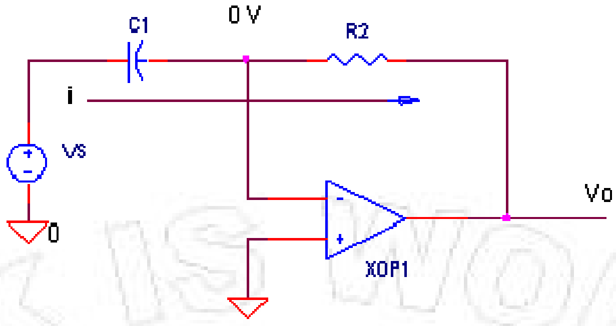
B) Differentitor **(5)**

ans: THE DIFFERENTIATOR



Its number one function is to create an output voltage proportional to the rate of change of the input voltage. This leads to applications such as extracting edges from square waves, converting sinewaves into cosines and changing triangle waves into square waves. But most circuits are susceptible to some trouble and this one's vulnerabilities are instability and noise. However, remedies are available to reduce the troubles without losing the desired function.

Ignoring R1 for a moment, let's look at the basic differentiator. How does this circuit respond to the rate of change of the input voltage?



the op amp's "prime directive" is to maintain 0 V (virtual ground) at its negative input. This places the input voltage VS across C1, producing an input current proportional to the rate of change of the input voltage.

$$i = C1 \cdot dVS / dt$$

Because no current flows into the op amp itself, *i* must flow through R2 creating the output voltage.

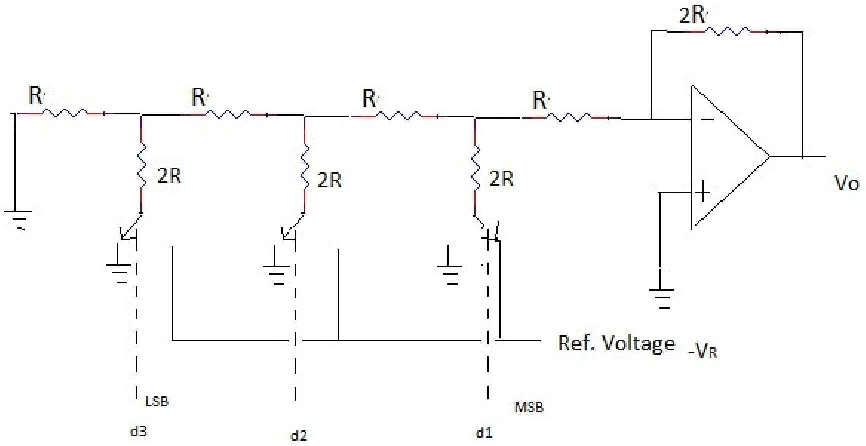
$$Vo = - i \cdot R2$$

Substituting for *i* we get

$$Vo = - C1 \cdot R2 \cdot dVS / dt$$

You may have noticed that the differentiator circuit looks a lot like its complementary companion, the integrator. The only difference being the swapped locations of the R and C

C) DAC using R-2R Resistors **(5)**



- Only 2 values of the resistors R and 2R.
- Switch positions are controlled by binary digital word d1d2d3 as shown in fig.
- Analog output voltage corresponding to each digital word is as shown in table.

Digital Input			Analog output voltage Vo
D1	D2	D3	
0	0	0	0
0	0	1	Vr/8

0	1	0	2Vr/8
0	1	1	3Vr/8
1	0	0	4Vr/8
1	0	1	5Vr/8
1	1	0	6Vr/8
1	1	1	7Vr/8

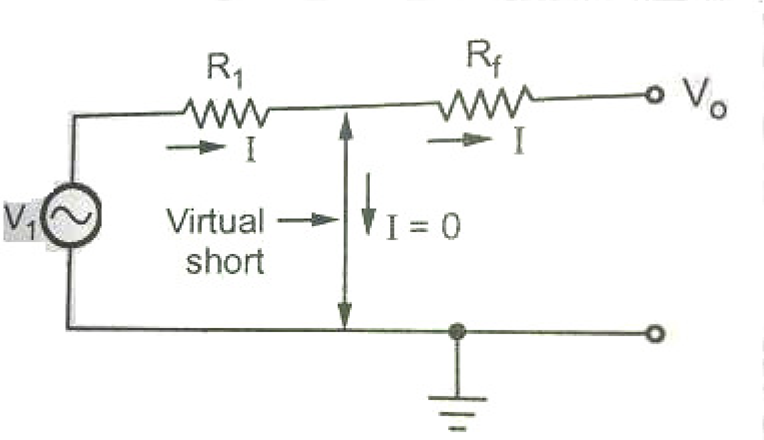
D) Virtual Ground of Op-Amp **(5)**

ans:

- The differential input voltage Vd between the non-inverting and inverting input terminals is zero
- This is because even if output voltage is few volts, due to large open loop gain of op-amp, Vd is almost zero.

Since Vo= Vd Aol
Vo/Aol = Vd
Vo/∞ =Vd
Vd=0

- As Vd= V1-V2
0= V1-V2
V1=V2



- Thus we can say that under linear range of operation there is virtually short circuit between 2 input terminals in the sense that their voltages are same. No current flows from input terminals to ground.
- The fig. shows the concept of virtual ground.
- Now if non-inverting terminal is grounded, by the concept of virtual short the inverting terminal is also at ground potential, though there is no physical potential between inverting terminal and ground.

This is the principal of Virtual Ground.

E) Inverting Schmitt Trigger **(5)**

ans: If the input to a comparator contains noise, the output may be erractive when v_{in} is near a trip point. For instance, with a zero crossing, the output is low when v_{in} is positive and high when v_{in} is negative. If the input contains a noise voltage with a peak of 1mV or more, then the comparator will detect the zero crossing produced by the noise. Fig. 1, shows the output of zero crossing detection if the input contains noise.

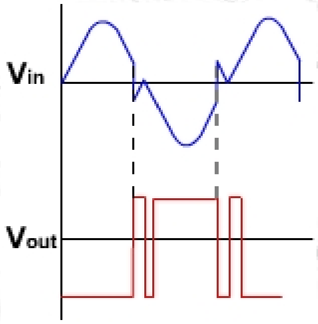


Fig. 1

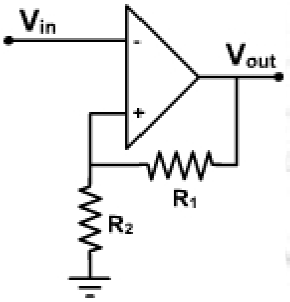


Figure 19.2

This can be avoided by using a Schmitt trigger, circuit which is basically a comparator with positive feedback. Fig. 2, shows an inverting Schmitt trigger circuit using OPAMP.

Because of the voltage divider circuit, there is a positive feedback voltage. When OPAMP is positively saturated, a positive voltage is feedback to the non-inverting input, this positive voltage holds the output in high stage. ($v_{in} < v_f$). When the output voltage is negatively saturated, a negative voltage feedback to the inverting input, holding the output in low state.

When the output is $+V_{sat}$ then reference voltage V_{ref} is given by

$$V_{ref} = \frac{R_1}{(R_1 + R_2)} * V_{sat} = (+\beta V_{sat})$$

If V_{in} is less than V_{ref} output will remain $+V_{sat}$.

When input v_{in} exceeds $V_{ref} = +V_{sat}$ the output switches from $+V_{sat}$ to $-V_{sat}$. Then the reference voltage is given by

$$V_{ref} = \frac{-R_2}{(R_1 + R_2)} * V_{sat} = (-\beta V_{sat})$$

The output will remain $-V_{sat}$ as long as $v_{in} > V_{ref}$.

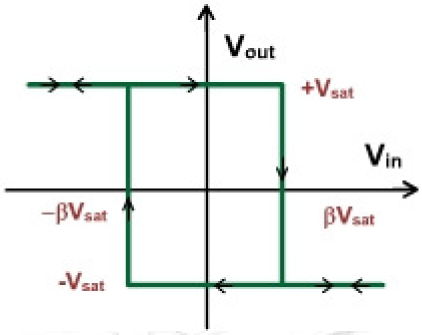


Fig. 3

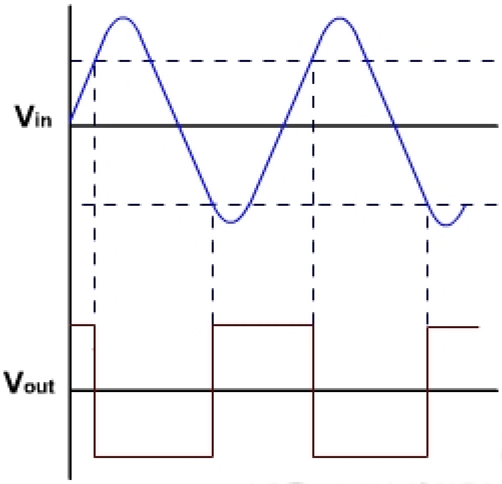


Fig. 4

If $v_{in} < V_{ref}$ i.e. v_{in} becomes more negative than $-V_{sat}$ then again output switches to $+V_{sat}$ and so on. The transfer characteristic of Schmitt trigger circuit is shown in fig. 3. The output is also shown in fig. 4 for a sinusoidal wave. If the input is different than sine even then the output will be determined in a same way.

Positive feedback has an unusual effect on the circuit. It forces the reference voltage to have the same polarity as the output voltage, The reference. voltage is positive when the output voltage is high ($+v_{sat}$) and negative when the output is low ($-v_{sat}$).

In a Schmitt trigger, the voltages at which the output switches from $+v_{sat}$ to $-v_{sat}$ or vice versa are called upper trigger point (UTP) and lower trigger point (LTP). the difference between the two trip points is called hysteresis.

$$UTP = \frac{R_2}{R_1+R_2} V_{sat}$$

$$LTP = \frac{R_2}{R_1+R_2} (-V_{sat})$$

$$V_{hys} = UTP - LTP$$

$$= \frac{R_2}{R_1+R_2} V_{sat} - \frac{R_2}{R_1+R_2} (-V_{sat})$$

$$= 2\left(\frac{R_2}{R_1+R_2}\right) V_{sat}$$

$$= 2\beta V_{sat}$$

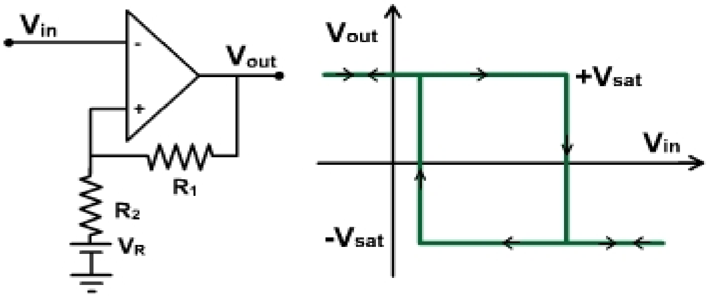


Fig. 5

The hysteresis loop can be shifted to either side of zero point by connecting a voltage source as shown in fig. 5.

When $V_O = +V_{sat}$, the reference. Voltage (UTP) is given by

$$\mathrm{UTP} = \frac{(V_{sat} - V_R)R_2}{R_1 + R_2} + V_R$$

$$= \beta V_{sat} + \frac{R_1 V_R}{R_1 + R_2}$$

When $V_O = -V_{sat}$, the reference. Voltage (UTP) is given by

$$\mathrm{LTP} = \frac{(-V_{sat} - V_R)R_2}{R_1 + R_2} + V_R$$

$$= -\beta V_{sat} + \frac{R_1 V_R}{R_1 + R_2}$$

If V_R is positive the loop is shifted to right side; if V_R is negative, the loop is shifted to left side. The hysteresis voltage V_{hys} remains the same.

Reference:	Electronic devices and linear circuits by Boylestad and Nashelsky Op-amp and linear circuits by Ramakant Gaikwad