

SUBJECT: DIGITAL LOGIC DESIGN

PAPER SOLUTION 2009-2010

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Q.NO.1)A) i) Convert $(43)_8 = (?)_{10} = (?)_2$

Ans:- $(43)_8 = (?)_{10} = (35)$

$$(43)_8 = (?)_2 = (100011)_2$$

ii) Find H if $(193)_H = (623)_8$.

$$X^2 + 9x + 3 = 384 + 16 + 3$$

$$X^2 + 9x + 3 = 403$$

$$X^2 + 9x - 400 = 0$$

$$X = 16.$$

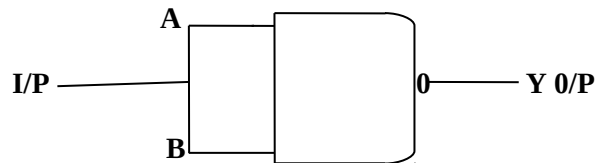
$$(193)_{16} = (623)_8.$$

Q.NO.1)B) Justify, NAND & NOR gates are universal logic gates.

Ans:- The NAND & NOR gate are called as universal gates because it is possible to

Implement any Boolean expression with the help of these gates.

e.g. NOT gate using NAND.



$$I/P \quad A=B=A.$$

$$Y = \overline{A \cdot B}$$

$$= \overline{A \cdot A}$$

$$= \overline{A}$$

Q.NO.1)C) Explain minterm & maxterm.

Ans:- Minterm:-

Each individual term in the standard SOP form is called as minterm.

$$\underbrace{ABC} + \underbrace{\overline{A}\overline{B}\overline{C}} + \underbrace{\overline{A}BC}$$

Each individual term is called minterm.

Maxterm:-

Each individual term in the standard POS form is called maxterm.

$$Y = \underbrace{(A + B)} \cdot \underbrace{(\overline{A} + \overline{B})}$$

Each individual term is called maxterm.

e.g. Let Y be the o/p & A, B, C, be the variables.

The number of minterm & maxterm is $2^3=8\dots$ 3=variables.

variables	minterm	maxterm
A B C	mi	mi
0 0 0	A B C=M0	A+B+C=M0
0 0 1	A B C=M1	A+B+C=M1
0 1 0	A B C=M2	A+B+C=M2
0 1 1	A B C=M3	A+B+C=M3
1 0 0	A B C=M4	A+B+C=M4
1 0 1	A B C=M5	A+B+C=M5
1 1 0	A B C=M6	A+B+C=M6
1 1 1	A B C=M7	A+B+C=M7

Q.NO.1)D) Compare TTL & ECL Logic families.

Ans:- PARAMETER	TTL Trans ^r trans ^r logic	ECL Emitter coupled logic.
Propagation delay	10ns.	500ps
Noise margin	0.4v.	150mv
Power dissipation	10mw.	5mw
Fan out	10	25

Fig.of merit

100pJ

0.5pJ.

Q.NO.2)A) Perform the following sequence.

i) $(10110.11)_2 \times (101.1)_2$.

Ans:-

$$\begin{array}{r} 10110.11 \\ \bullet \quad 101.1 \\ \hline 1011011 \\ 10110110 \\ 00000000 \\ 1011011000 \\ \hline 1111101001 \end{array}$$

ii) $(234)_{10} \times (12)_{10}$.

Ans:- Not possible

iii) $(CA)_{16} \times (6E)_{16}$.

Ans:- CA = 1100 1010.

6E = 0110 1110.

: $(CA)_{16} \times (6E)_{16} = 56CC$.

iv) $(23 - 48)_{10}$ - using 2's complement.

Ans:- $(23)_{10} = 010111$

$(48)_{10} = 110000$

Is complement of 48 = 001111

2's complement = + 11111

010000

23 = 010111

+ 010000

0100111

100111

- 1

200110

$$: 011001 = (-25)_{10}$$

Q.NO.2)B) I) Explain different between weighted codes & nonweighted codes.

Ans:- Weighted binary codes:-

- i) Positional weight principle.
- ii) Each position of the number represents a specific weight.
- iii) 8421,2421,3321 all are the weighted codes.

Non weighted codes:-

- i) Positional weights are not assigned.
- ii) E.g:- non weighted codes are excess-3 & gray codes.

II) Perform $(54)_{10} - (22)_{10}$ in BCD using 10's complements.

Ans:- 9's complements = 22.

$$99 - 22 = 77$$

$$10\text{'s complements} = 77 + 1 = 78$$

$$(54)_{10} = 01010100$$

$$(78)_{10} = 01111000$$

$$\underline{11001100}$$

$$\text{Invalid BCD} = 01100110$$

$$1 \quad \underline{0011} \quad \underline{0010}$$

$$3 \quad 2$$

Q.NO.3)A) Implement using only NAND & NOR.

$$F (0,1,2,3,8,9,12,13,14)$$

Ans:- $I (A,B,C,D) = F (0,1,2,3,8,9,12,13,14)$

$$Y = \overline{A} \overline{B} + \overline{C} A + A B \overline{D}$$

Use demorgan's th^m.

$$Y = A B + C A + A B D$$

$$= A B . C A . A B D$$

$$Y = A B + C A + A B C D$$

$$Y = P + Q + R$$

$$Y = P + Q + R$$

$$= P.Q.R$$

$$P = A B = A + B$$

Q

$$Y = (A + B)(A + C)(A + B + D)$$

$$= (A + B) + (A + C) + (A + B + D)$$

$$Y = A + B + (A + C) + (A + B + D)$$

$$Y = A + B + A + C + A + B + D.$$

Q.NO.3)B) Reduce using Quine Mcciuskey & implement using logic gates.

Ans:- I) $F(A,B,C,D) = \sum M(2,3,6,7,8,9,13,15) + d(4,10,12)$

Group	minterm	Binary representation.			
		A	B	C	D
0	2	0	0	1	0
1	3	0	0	1	1
2	6	0	1	1	0
3	7	0	1	1	1
4	8	1	0	0	0
5	9	1	0	0	1
6	13	1	1	0	1
7	15	1	1	1	1
8	4*	0	1	0	0
9	10*	1	0	1	0
10	12*	1	1	0	0

II) According to no.1's.

Group	Minterm	Binary presentation			
0	2	0	0	1	0
	4	0	1	0	0 one 1's
	8	1	0	0	0
1	3	0	0	1	1
	6	0	1	1	0 Two 1's
	9	1	0	0	1
	10*	1	0	1	0
	12*	1	1	0	0
2	7	0	1	1	1 Three 1's
	13	1	1	0	1
3	15	1	1	1	1 Four 1's

III) Group minterms to form pairs.

Group	min.pairs	Binary representation.			
		A	B	C	D
0	2-3	0	0	1	-
	2-6	0	-	1	0
	2-10*	-	0	1	0 B C D
	4*-6	0	1	-	0 A B D
	4-12*	-	1	0	0 B C D
	8-9	1	0	0	-
	8-10*	1	0	-	0 A B D
	8-12*	1	-	0	0
1	3-7	0	-	1	1

	6-7	0	1	1	-	
	9-13	1	-	0	1	
	12*-13	1	1	0	-	
2	7-15	-	1	1	1	B C D
	13-15	1	1	-	1	A B D

IV) Group the minterms to from group of 4.

Group	Minterm Quad.	Binary representation.			
		A	B	C	D
0	2,3,6,7	0	-	1	- } A C
	2,6,3,7	0	-	1	- } Prime
	8,9,12,13	1	-	0	- } A C
	8,12,9,13	1	-	0	- } Implication

V) Prepare table of P.I.

P.I	Dec.No.	Minterms given.							
		2	3	6	7	8	9	15	
B,C,D	2,10	*							
A,B,D	4,6			*					
B,C,D	4,12								
A,B,D	8,10					*			
B,C,D	7,15				*			*	
A,B,D	13,15								*
A,C	2,3,6,7	*	*	*	*				
A,C	8,12,9,13					*	*		

The encircles crosses represents the essential P.I. A C & A C covers minterms 2,3,6,7,8,9,12,13 But 15 is not covered.

The P I A B D covers this term.

$$F (A,B,C,D) = A B D + A C + A C.$$

Implimentation:-

Q.NO.4)A) Implement a 16:1 MUX using 4:1 MUX.

Ans:- i) Given MUX = 4:1

Select lines = 2.

i/p lines = 4.

o/p line = 1

ii) The select i/p's s1 & s0 of MUX 1,2,3,4.

Total MUX = Required MUX size

Available MUX size

= 16 : 1

4 : 1

= 4 MUX:5

iii) 16 : 1 MUX.

Select lines = 4.

i/p lines = 16.

o/p lines = 1.

S0,S1,S2,S3 are select lines.

S3 & S2 are applied to select i/p's S1 & S0 of MUX.

iv) The o/p Y1,Y2,Y3,Y4 are applied to data i/p's D0,D1,D2 & D3 of MUX 5

v) T.T.

Selectb i/p's MUX o/p's final o/p.

S3	S2	S1	S0	Y1	Y2	Y3	Y4	Y
0	0	0	0	D0	D4	D8	D12	D0
0	0	0	1	D1	D5	D9	D13	D1
0	0	1	0	D2	D6	D16	D14	D2
0	0	1	1	D3	D7	D11	D15	D3
0	1	0	0		D4			D4
0	1	0	1		D5			D5
0	1	1	0		D6			D6
0	1	1	1		D7			D7
1	0	0	0			D8		D8
1	0	0	1			D9		D9
1	0	1	0			D10		D10
1	0	1	1			D11		D11
1	1	0	0				D12	D12
1	1	0	1				D13	D13
1	1	1	0				D14	D14
1	1	1	1				D15	D15

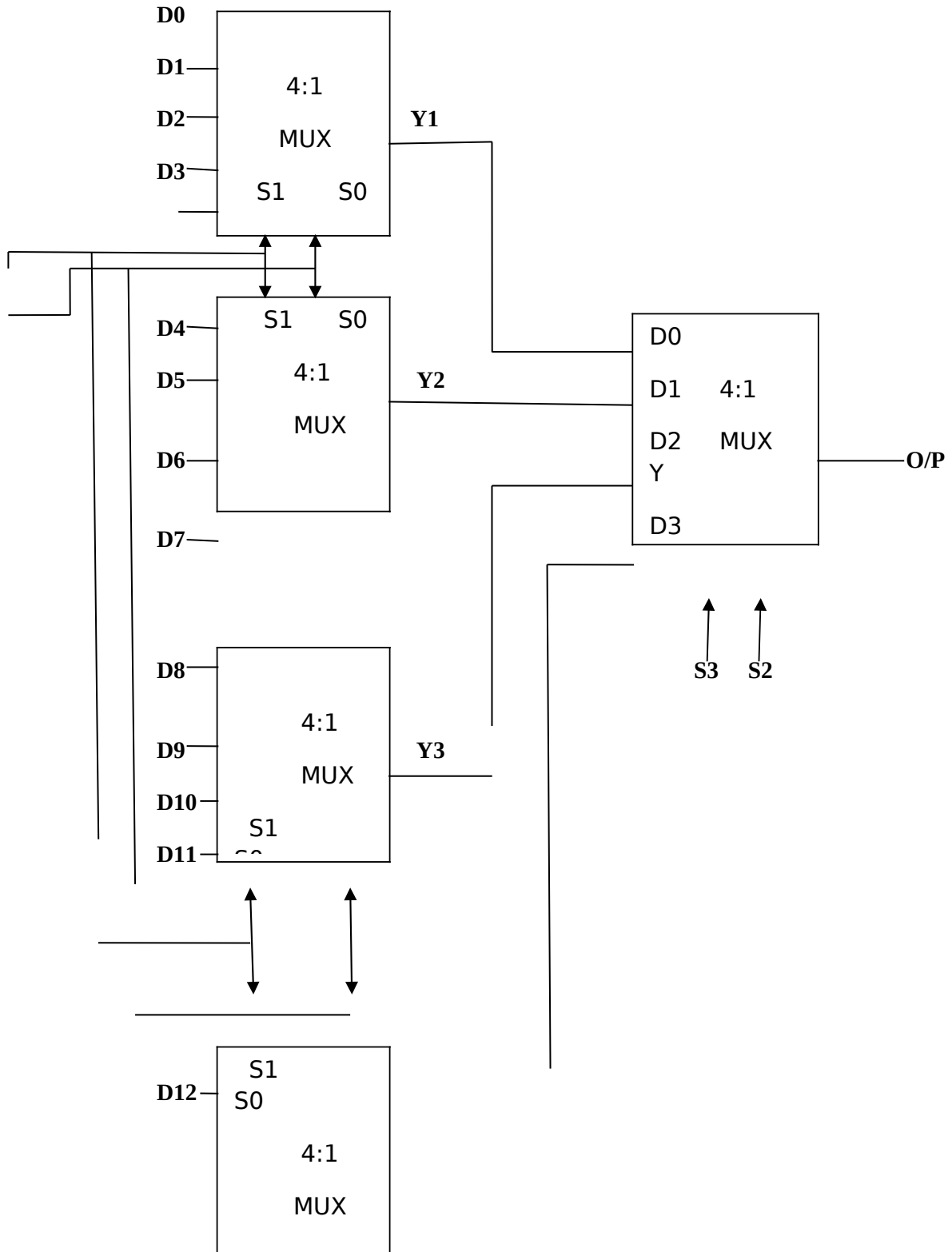
S3S2=00
MUX.5
Select Y1

S3S2=01
Select Y2

S3S2=10
Select Y3

S3S2=11
Select Y4

Implementation:



D13—

Y4

D14—

D15—

Q.NO.4) B) Design a combinational circuit using PAL for

$$W(A,B,C,D) = \sum M(2,12,13)$$

$$X(A,B,C,D) = \sum M(7,8,9,10,11,12,13,14,15)$$

$$Y(A,B,C,D) = \sum M(0,2,3,4,5,6,7,8,10,11,15)$$

$$Z(A,B,C,D) = \sum M(1,2,8,12,13)$$

Equation:

A

	01	11	10	
A			1	→ ABCD
B				
C				
D				

C

BCD

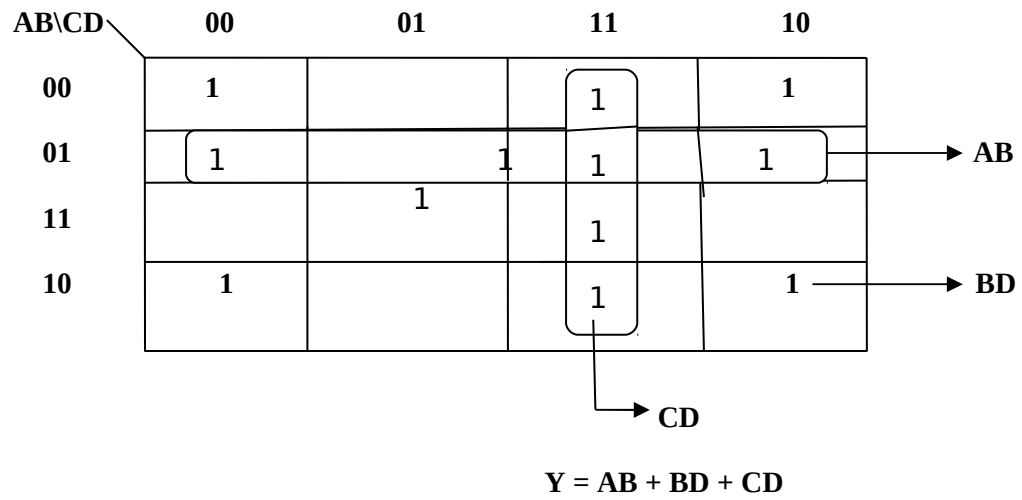
		11	10	
A				→ BCD
B		1		
C		1	1	
D	1		1	

10

→ A

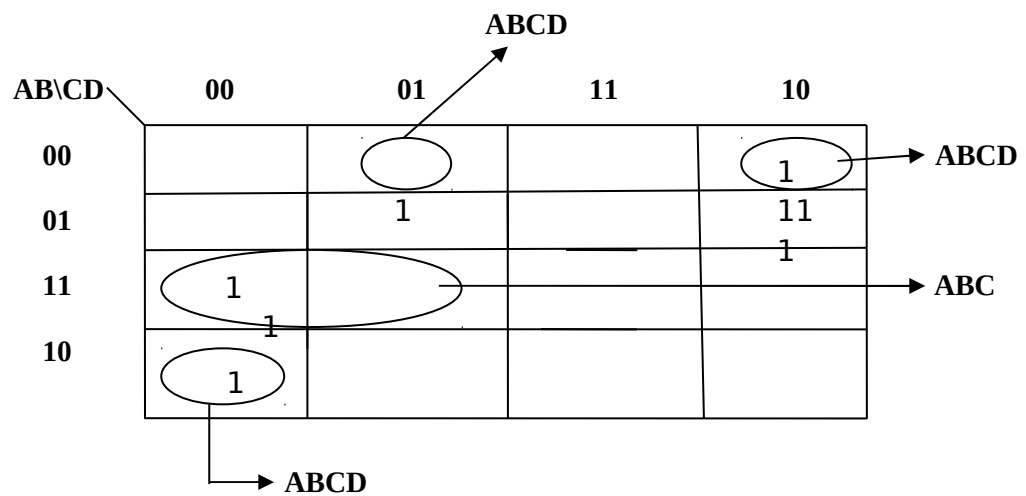
$$X = A + BCD$$

For - Y



❖

For - Z



$$Z = ABCD + \underbrace{ABCD + ABC + ABCD}_W$$

$$Z = W + ABCD + ABCD$$

Step:2:- PAL Programming table:-

Product term no.	product term	AND inputs	outputs
		A B C D W	
1	ABC	1 1 0 - -	w=ABC+ABCD
2	ABCD	0 0 1 0 -	
3	-	- - - - -	
4	A	1 - - - -	x=A + BCD
5	BCD	- 1 1 1 -	
6	-	- - - - -	
7	AB	0 1 - - -	y = AB + BD + CD
8	BD	- 0 - 0 -	
9	CD	- - 1 1 -	
10	W	- - - - 1	z = W +ABCD+ABCD
11	ABCD	0 0 0 1 -	
12	ABCD	1 0 0 0 -	

Table P. 7.4.1 : PAL programming table

Product term No.	Product term	AND inputs					Outputs
		A	B	C	D	w	
1	$\overline{B}D$	-	0	-	1	-	$w = \overline{B}D + B\overline{D}$
2	$B\overline{D}$	-	1	-	0	-	
3	w	-	-	-	-	1	$x = w + ABC$
4	ABC	1	1	1	-	-	
5	$\overline{C}D$	-	-	0	0	-	$y = \overline{C}D + AD$
6	$\overline{A}D$	0	-	-	1	-	
7	$\overline{A}C$	1	-	0	-	-	$z = \overline{A}C + A\overline{B}C$
8	$\overline{A}B\overline{C}$	0	0	1	-	-	

Step 3 : Logic diagram :

The logic diagram is as shown in Fig. P. 7.4.1(e).

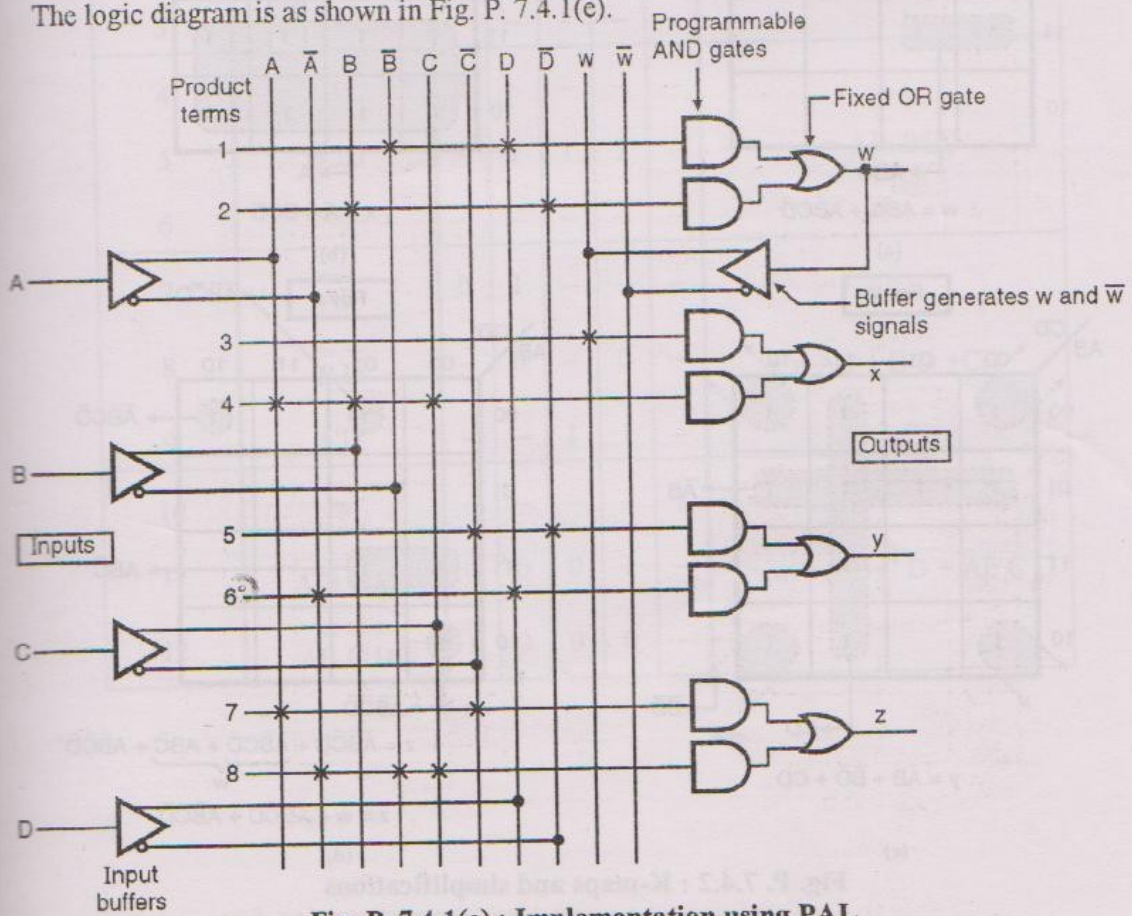
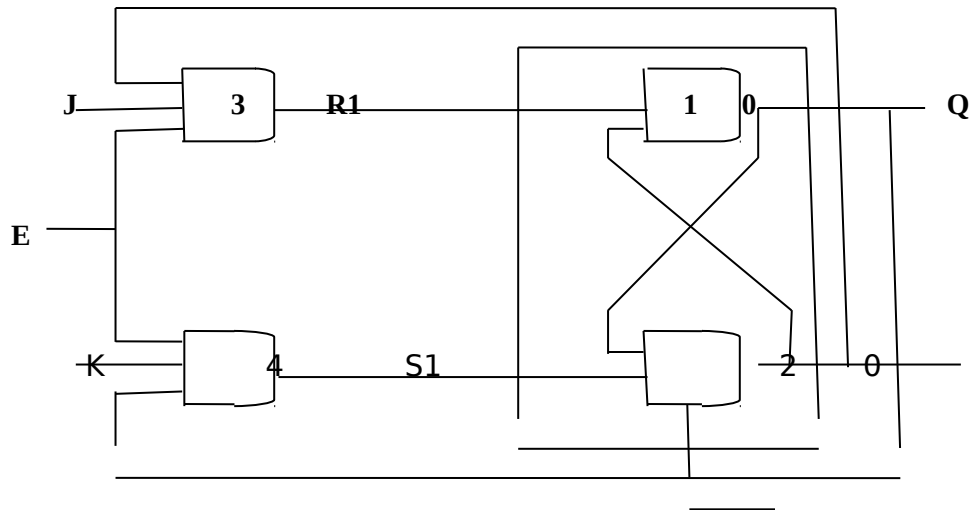


Fig. P. 7.4.1(e) : Implementation using PAL

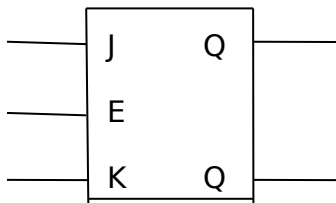
Q.NO.5)A) Explain J.K.latch using NAND gates.



Q

Basic

SR latch



It consists of the basic SR latch.& enable i/p.

Truth Table:-

Case no.	I/p's			o/p's			state
	E	J	K	Q _{n+1}	Q _{n+1}	No change	
Case.I	0	X	X	Q _n	Q _n	N.C	
Case.II		1	0	0	1	Reset	
Case.III		1	1	1	0	Set	
Case.IV		1	1	1	1	Toggle.	

Explanation:-

Design a sequence detector to detect the following sequence using D flip-flops. ... 110 ...

Draw the state diagram :

The state diagram is as shown in Fig. P. 11.17.2(a).

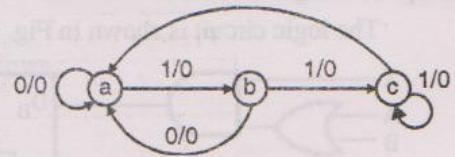


Fig. P. 11.17.2 (a) : State diagram

Write the state table :

Table P. 11.17.2(a) : State table

Present state	Next state		Output	
	X = 0	X = 1	X = 0	X = 1
a	a	b	0	0
b	a	c	0	0
c	a	c	1	0

Assign states :

The assignment is carried out in the normal binary sequence as follows :

$$a = 00, \quad b = 01, \quad c = 10.$$

Write the circuit excitation table :

Table P. 11.17.2(b) : Circuit excitation table

Input X	Present state		Next state		F/F inputs		Output Y
	B	A	B ₊₁	A ₊₁	D _B	D _A	
0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0
0	1	0	0	0	0	0	1
0	1	1	X	X	X	X	X
1	0	0	0	1	0	1	0
1	0	1	1	0	1	0	0
1	1	0	1	0	1	0	0
1	1	1	X	X	X	X	X

Groups and simplifications :

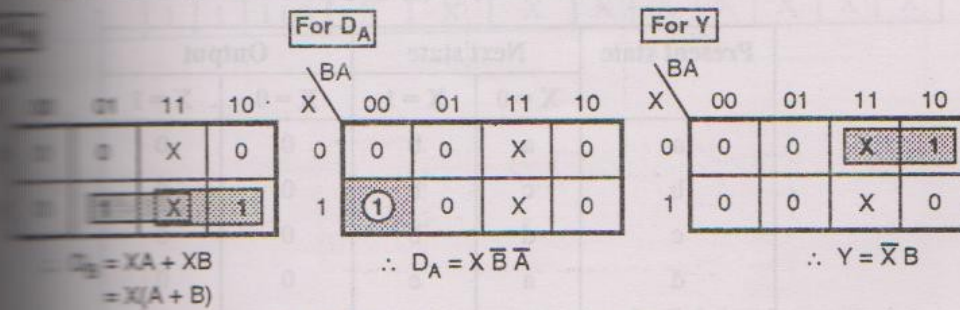


Fig. P. 11.17.2 (b) : K-map and simplifications

Step 6 : Logic circuit :

The logic circuit is shown in Fig. P. 11.17.2(c).

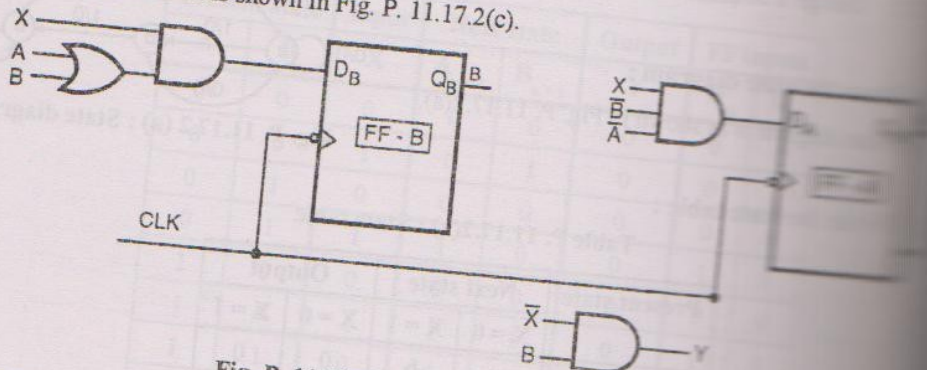
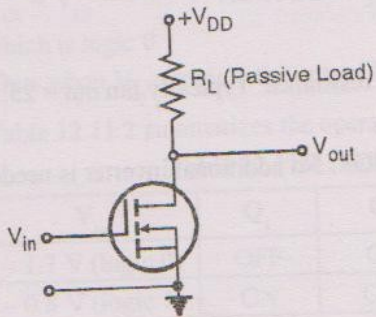


Fig. P. 11.17.2(c) : Logic circuit of the

7)A

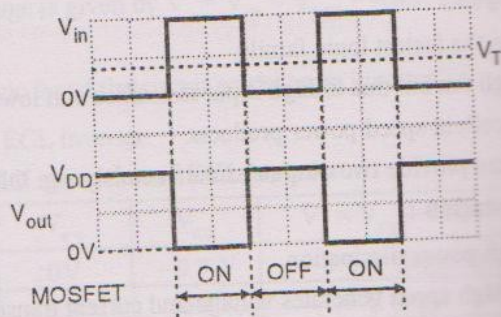
7)B

MOSFET operates as a switch. Fig. 12.12.2(a) shows the passive load circuit acting as a passive load.



(a) Passive load switching circuit

Fig. 12.12.2



(b) Waveforms

12.12.5 A PMOS Inverter :

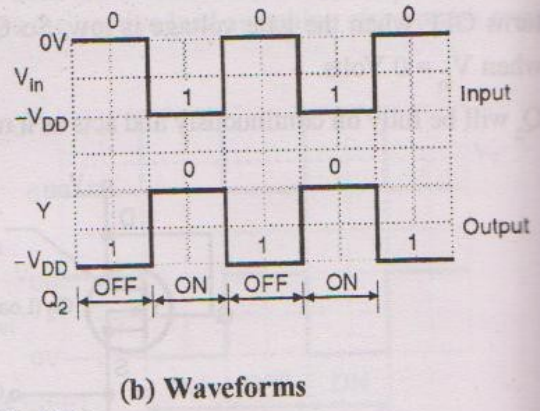
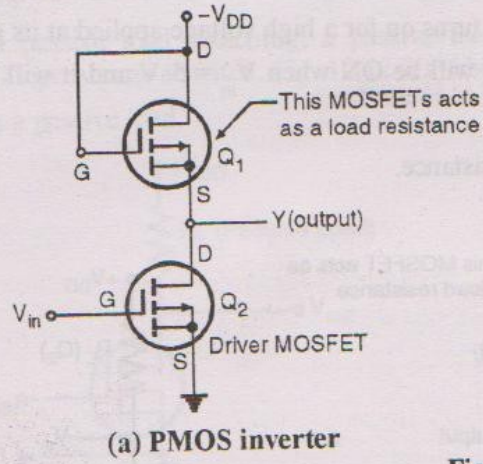
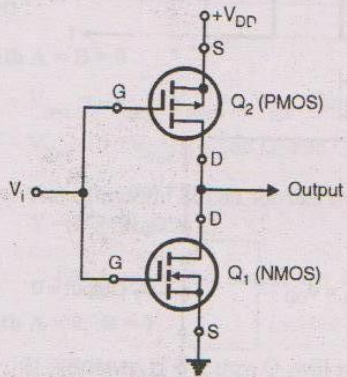


Fig. 12.12.5

input TTL gate in the 7400 TTL family.

2.13.1 CMOS Inverter :



V _i	Q ₁	Q ₂	Output
0V (logic 0)	OFF	ON	V _{DD} (logic 1)
V _{DD} (logic 1)	ON	OFF	0 (logic 0)