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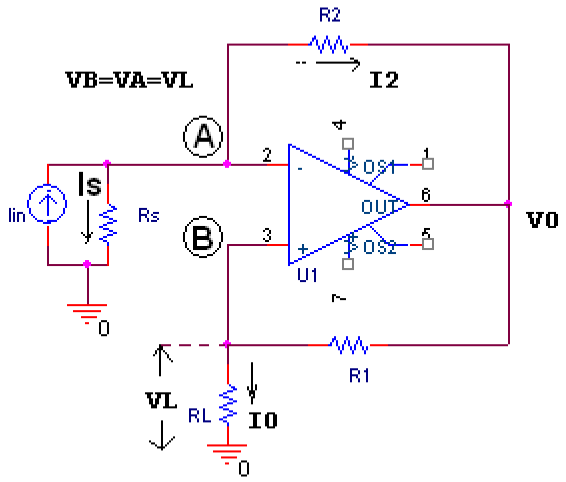
Examination:- Win -2010 SEM-IV, SE -EXTC (Revised)

Subject:- ADIC & DA

Question Paper code no. GT-6516

Q.1) Analyze the current amplifier with grounded load.



Applying KCL at Node B,

$I_{in} = I_s + I_2$

$I_2 = I_{in} - I_s = I_{in} - (V_B/R_s)$

$V_B = V_A = V_L$

Output voltage of op-amp is given by,

$V_0 = V_B - I_2 \chi R_2$

$Vo = V_L - [I_{in} - (V_L/R_s)] \chi R_2$

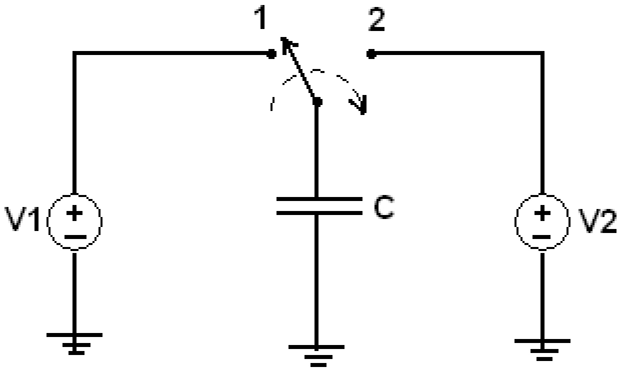
$$I0 = \frac{Vo - VL}{R1}$$

But $Io = -\frac{R2}{R1} \square\, Iin - \frac{VL}{R1}[-1 - \frac{R2}{Rs} + 1]$

$$I0 = -\frac{R2}{R1} \square\, Iin - [\frac{R2}{R1 \square\, Rs}] \square\, VL$$

Basically op-amp is voltage amplifier device, but we can configure them to amplify current.

Q.2) How switched capacitor can simulate resistor?



When switched is in position-1, capacitor charges up to V1, and when it is in position-2, capacitor discharge to V2

*** Net charge transfer from V1 to V2 is given.

$\Delta Q = C(V1 - V2)$

*** If switching rate is adjusted to a rate of f_{CLK}

$$Iavg = \frac{\Delta Q}{Sec} \quad \text{but 1 Sec= 1/ } f_{CLK}$$

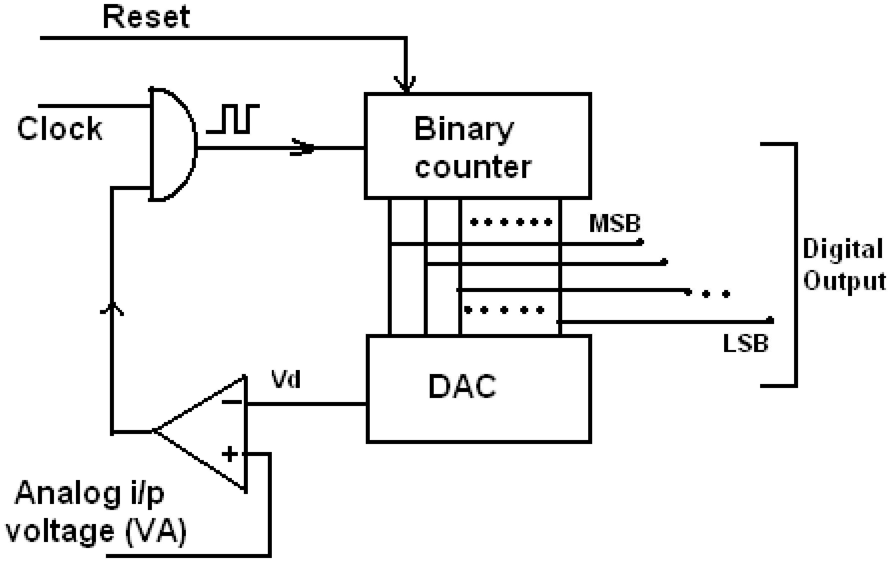
$$Iavg = \Delta Q \times fclk = C(V1 - V2) \times fclk$$

*** hence equivalent resistance is given by

$$\mathrm{Re}\,q = \frac{V1 - V2}{Iavg} = \frac{V1 - V2}{C(V1 - V2) \times Fclk}$$

$$\mathrm{Re}\,q = \frac{V1 - V2}{Iavg} = \frac{1}{C \times fclk}$$

C) With neat circuit diagram, explain counter type A-to-D converter.



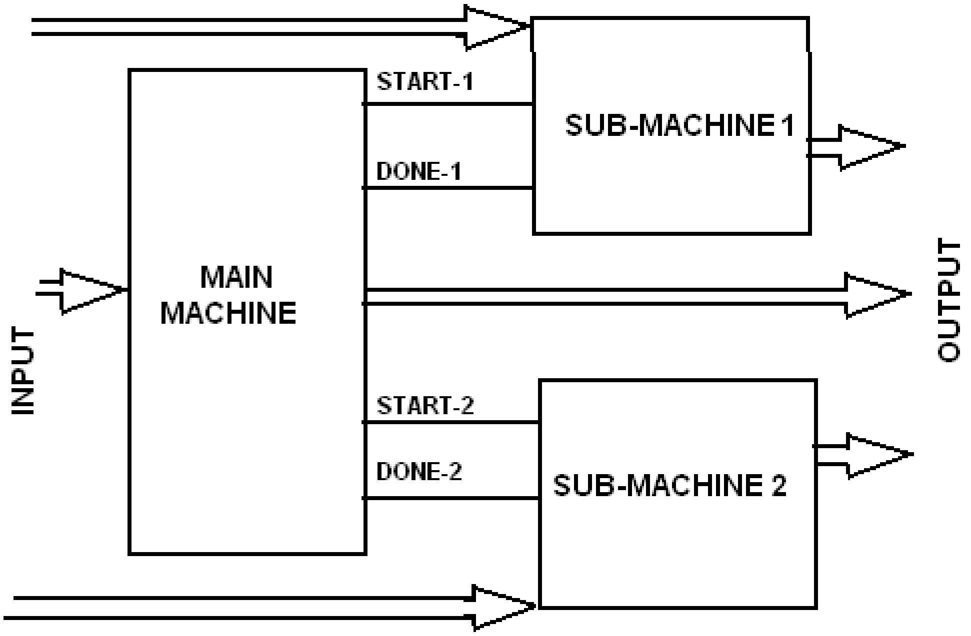
Counter is reset to zero, by applying reset pulse. After applying reset, pulses are applied through AND gate.

- Initially DAC is zero. Therefore analog input Va is higher than the DAC output (Va > Vd). Therefore comparator output is high and ABD gate is enabled. Thus clock pulse are allowed to pass through AND gate to counter.
- Counter start counting these pulses. As counter output acts as input to DAC, DAC output also increases.
- As long as Vd < Va, this process will continued, as comparator output remains high, enabling the AND gate.
- However as soon as DAC output is higher than input analog voltage Va < Vd, comparator output becomes low. This process will disable AND gate and stop the clock pulses. Digital output of the counter represents analog output.

D) Differentiate between SRAM and DRAM

	SRAM	**DRAM**
1	Cell of the SRAM is flip-flop.	DRAM unit consists of one MOSFET and capacitor.
2	Number of component per cell is more.	Number of component per cell is low.
3	Memory per area is less.	Memory per area is more.
4	Refreshing is not required.	Refreshing circuit is required.
5	Access time is less, so that this is faster.	Access time is more, so that this is slower.

E) Explain state machine decomposition.



Many times it's not configurable to design a huge machine, because of many variables changing at a times or different time. So that while doing programming main routine has to be divided in to small sub-routine. To decompose the state machine following steps are used—

- Main machine provides primary input and output.
- Main machine execute top level control algorithm.
- Sub-machine performs lower level steps.
- Sub-machine is under control of main machine.
- Sub-machine may optionally handle some of primary input and output.

Above process of breaking of total machine into main machine and sub-machine is referred as state machine decomposition.

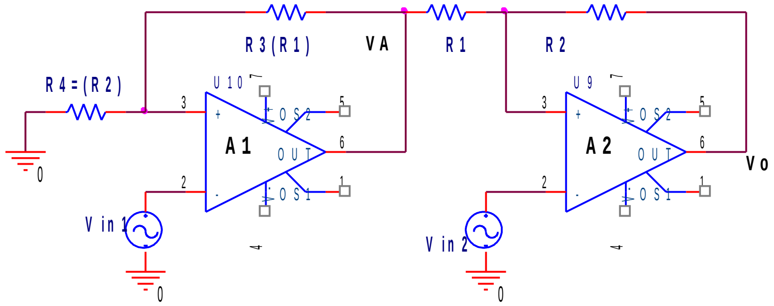
Q.2)

a) Draw a neat circuit diagram of an instrumentation amplifier using three op-amp. Derive its output voltage equation.

-In industrial application measurement and control quality are required such as temperature, pressure and humidity etc. transducer is used to convert this quantity into electrical quantity proportionally. Output of transducer is then applied to an amplifier which is called as "instrumentation amplifier".

* Advantages of instrumentation amplifier*

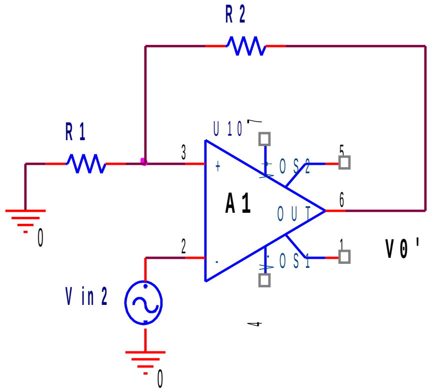
- **Precise low level signal amplification:-** Instrumentation amplifier are expected to amplify the signal of very small amplitude. Therefore gain should be high and accurate.
- **Low noise:-** Basically I.A. is differential amplifier so that noise is low.
- **Variable gain**:- With resistance R2, gain of I.A. can be varied precisely.
- **High i/p impedance:-** Input impedance of I.A. is very high, because it is depending on two unity buffer amplifier.
- **Low o/p Impedance:-** Output impedance of amplifier is decided by the amplifier A3.



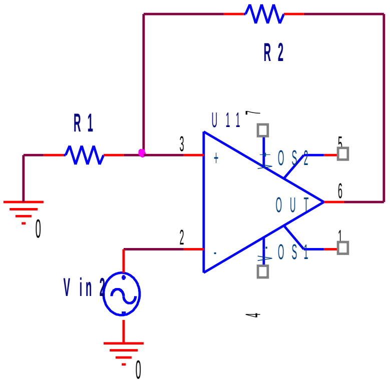
A1 is a non-inverting amplifier hence its output voltage is given by

$$V01 = [1+\frac{R3}{R4}]\cdot Vin1$$

V01 is applied to the inverting terminal of A2. Hence its output voltage V0 can be obtained with the help of superposition theorem by considering V01 and Vin2 separately as shown in figure.



A2 acts as an inverting amplifier with gain of R2/R1



A2 acts as an non-inverting amplifier with gain of 1+R2/R1

Output voltage V0' by considering only V01 as shown in figure is given by

$$Vo' = -\frac{R2}{R1}\cdot Vo1 = -\frac{R2}{R1}\cdot(1+\frac{R3}{R4})\cdot Vin1$$

And output voltage Vo'' by considering only Vin2 as shown in figure is given by

$$Vo'' = [1+\frac{R2}{R1}]\cdot Vin2$$

Hence output voltage V0=Vo'+Vo''

Substituting the values we get,

$$Vo = -\frac{R2}{R1}\cdot[1+\frac{R3}{R4}]Vin1 + [1+\frac{R2}{R1}]Vin2$$

$$Vo = [1+\frac{R2}{R1}]Vin2 - [\frac{R2}{R1}(1+\frac{R3}{R4})]Vin1$$

Take out 1+(R2/R1) common from the first RHS of expression Vo to obtain,

$$Vo = 1+\frac{R2}{R1}(Vin2 - \frac{1+(R3/R4)}{1+(R1/R2)}Vin1)$$

The circuit will work as a true difference amplifier if

$$\frac{R1}{R2} = \frac{R3}{R4} \text{ or } 1+\frac{R1}{R2} = 1+\frac{R3}{R4}$$

When this condition is satisfied equation reduced to

$$V0=[1+\frac{R2}{R1}]\square(Vin2-Vin1)$$

The circuit has the advantage of high input impedance and low output impedance.

b) Lists different commercial ROM types. Differentiate them.

- Mask programmable ROM
- Programmable ROM
- Erasable Programmable ROM
- Electrical erasable programmable ROM

Mask programmable ROM

In this data pattern must be programmed as a part of manufacturing process.
It is not programmable.
Normally it is used for high volume usage due to low cost.

Programmable ROM

This device is electrically programmable. Here user can program this chip.
Normally PROM is one time programmable.

Erasable programmable ROM

In this memory data can be written any number of times.
Chip can be erased by exposing it to UV rays called EPROM.
This is used when one want to develop digital computer system.

Advantage:

- Can be reprogrammed so useful for field upgrades, debug trials.

Disadvantages:

- The whole contents need to be erased, selective erasure not possible
- Over-exposure to UV rays may damage the device.

Use:

It is used for device boot-up, lookup tables. (Though EPROMs are extinct and replaced by EPROMS)

Electrically erasable programmable ROM

To erase particular location a voltage of 20 to 25V is applied.
Selective location can be erased, which is not possible in EPROM.
Few milliseconds are required to erase data.
To erase the ROM it is not necessary to remove PROM from circuit.

Advantages:

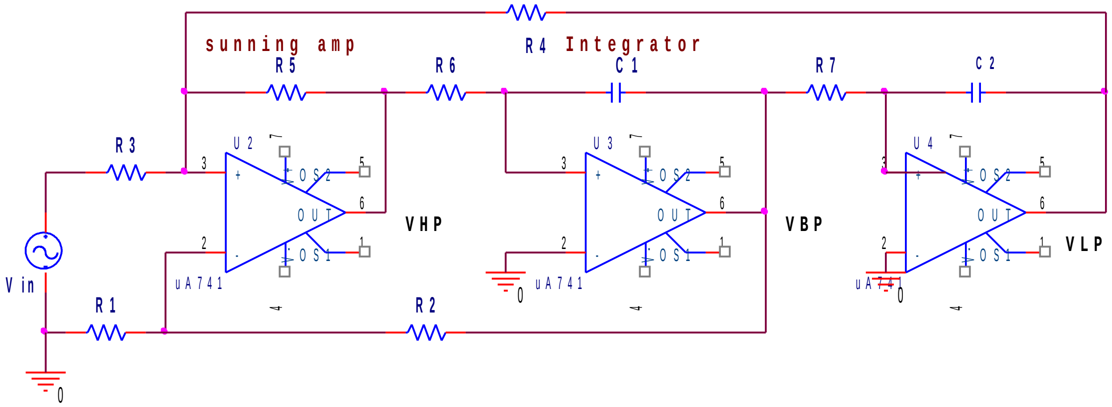
- The chip does not have to be removed to rewrite.
- The entire chip does not have to be completely erased to change a specific portion of it.
- Changing the contents does not require additional dedicated equipment.

Q.3)

a) What are the universal filters? Draw neat circuit diagram of any universal filter and find out its output voltage equation.

Multiple op-amp filter such as state-variable and Bi-quad filter are called as universal filter. Because, they simultaneously provides more than one frequency response.

Figure shows state variable circuit which provides the second order low pass, band pass, and high pass response simultaneously.



We can obtain the output of A1 by mean of using the principle of superposition by considering every input to A1 separately and assign their response as follows.

Output of A1= $V_{HP}=-\frac{R5}{R3}\cdot Vin-\frac{R5}{R4}\cdot VLP+[1+\frac{R5}{R3\parallel R4}]\cdot\cdot\frac{R1}{R1+R2}\quad VBP$

A2 and A3 are integrator hence their output are

Output A2=V_{BP}=voltage across C_1

$$V_{BP}=-\frac{1}{s\cdot C1\cdot R6}\cdot VHP$$

And Output A3=V_{LP}=Voltage across C2

$$V_{LP}=-\frac{1}{s\cdot C2\cdot R7}\cdot VBP$$

Now substituting the expression for V_{HP} from above equation and rearrange the term we get—

$$\frac{VHP}{Vin}=-\frac{R5}{R3}\cdot\frac{R4\cdot R6\cdot C1\cdot R7\cdot C2\cdot S^{2}/R5}{R4\cdot R6\cdot C1\cdot R7\cdot C2\cdot S^{2}/R5+\{R4(1+\frac{R5}{R3}+\frac{R5}{R4})\cdot s/(1+R2/R1)R5+1\}}$$

But we know that standard 2nd order HPF

$$HHP(jw)=\frac{-(w/w0)^{2}}{1-(w/w0)^{2}+(jw/w0)/Q}$$

$$w0=\frac{\sqrt{R5/R4}}{\sqrt{R6\cdot C1\cdot R7\cdot C2}}\qquad Q=\frac{(1+\frac{R2}{R1})\sqrt{\frac{R5\cdot R6\cdot C1}{R4\cdot C2\cdot R7}}}{1+\frac{R5}{R3}+\frac{R5}{R4}}$$

We know that, $V_{BP}=-\frac{1}{s\cdot C1\cdot R6}\cdot VHP$

Dividing both sides by Vin, we get,

$$\frac{VBP}{Vin} = H_{OHP} \cdot H_{BP}$$

This allows us to obtain the value of H_{OBP} as

$$H_{OBP} = \frac{1 + R2/R1}{1 + R3/R4 + R3/R5} \quad \text{and} \quad H_{OHP} = -\frac{R5}{R3}$$

Simplifying $V_{LP} = -\frac{1}{S \cdot C2 \cdot R7} \cdot V_{BP}$

Dividing both sides by Vin we get,

$$\frac{V_{LP}}{Vin} = -\frac{1}{S \cdot C2 \cdot R7} \cdot \frac{V_{BP}}{Vin}$$

We can get

$$H_{OLP} = -\frac{R4}{R3}$$

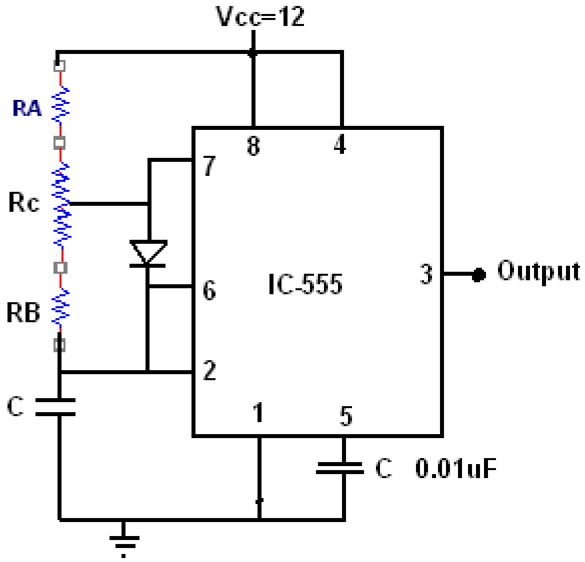
B) Write VHDL program for 4-bit decade counter with enable, reset and synchronous clock input.

```
Library ieee;
Use ieee.std_logic_1164.all;
Use ieee.std_logic_unsigned.all;

Entity decade is
        Port( clk, en, reset : in std_logic;
                             Q : Out std_logic_vector(std_logic_vector(3 downto 0));
End decade;

Architecture a_decade of decade is

Signal temp : std_logic_vector(3 downto 0);

Begin
Process(clk, reset)
 Begin
  If(clk=’1’ and clk’event) then
        If (reset=’0’) then
         Temp <= “0000”;
        Else
        If(en=’1’) then
                If(temp < 9) then
                      Temp <= temp + “0001”;
                Else
                      Temp <= “0000”;
                End if;
        End if;
        End if;
End if;
End process;
```

```
Q <= temp;

End a_decade;
```

Q.4)

a) Design an astable multivibrator for an output frequency of 1 KHz but a variable duty cycle of 30 % to 70 %. Assume V_{CC}=12V.



Time of one cycle **=** 1/frequency
= 1/1 KHz
= 1000uSec

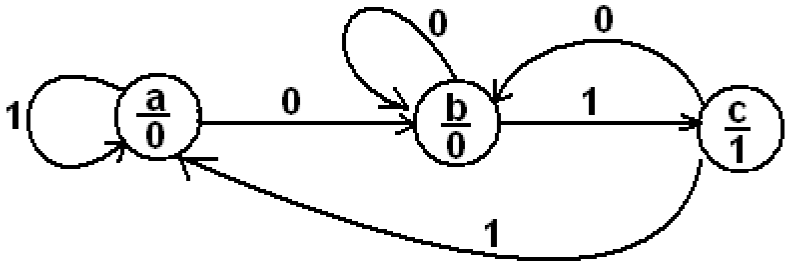
T_{ONmin}=300uSec T_{OFFMax}=700uSec
T_{ONmax}=700uSec T_{OFFMin}=300uSec

T_{ONmin}=0.693*(R_A)*C=300uSec
Assume C=0.1 uF
R_A=4.329KΩ

T_{ONMax}=0.693*(R_A+R_C)*C=700uSec
Rc=5772.0Ω= 5.772KΩ
T_{ONMin}=0.693*R_B*C=300uSec
R_B=4.329KΩ

b) Design a logic circuit that asserts its output for one cycle when the input stream changes from 0 to 1 using (i) Moore Machine (ii) Melay machine.

i) Moore machine:-

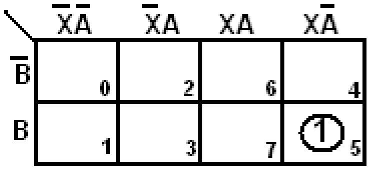


Assume a=00;
b=01;
c=10;

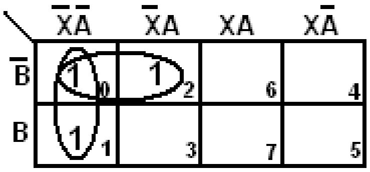
State table:-

X	A	B	A+	B+	Y
0	0	0	0	1	0
0	0	1	0	1	0
0	1	0	0	1	1
0	1	1	0	0	0
1	0	0	0	0	0
1	0	1	1	0	0
1	1	0	0	0	1
1	1	1	0	0	0

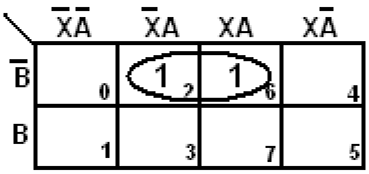
We will use D-FF



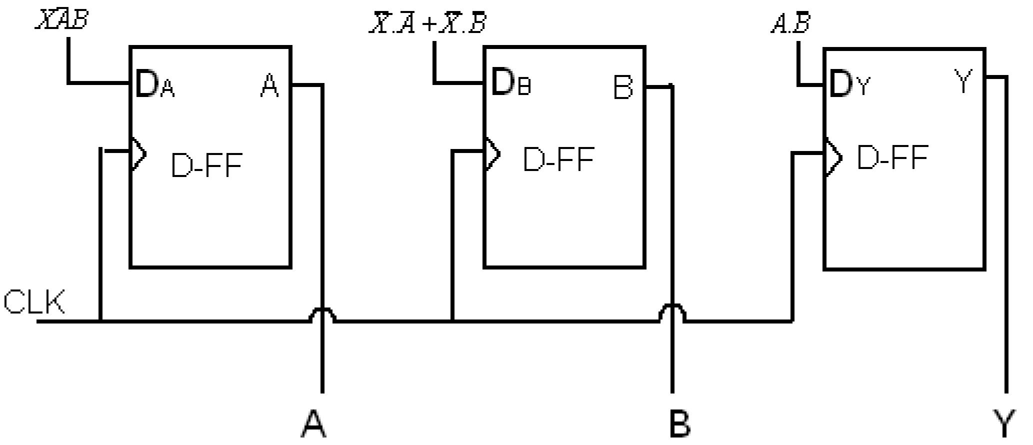
A+= $X\bar{A}B$



B+= $\bar{X}.\bar{A} + \bar{X}.\bar{B}$

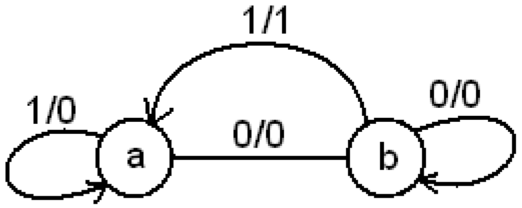


Y= $A.\bar{B}$



ii) Melay machine:-

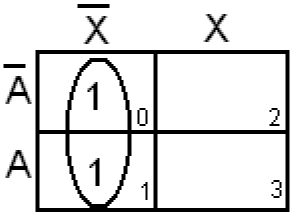
we will detect the sequence ……01…..



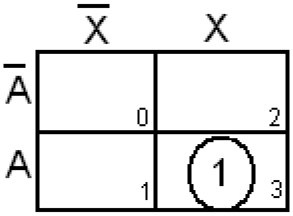
Assume states a=0 and b=1

State table

X	A	A+	Y
0	0	1	0
0	1	1	0
1	0	0	0
1	1	0	1

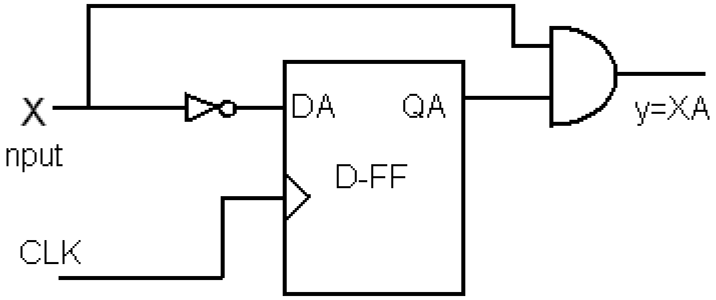


A+= $\overline{X}$

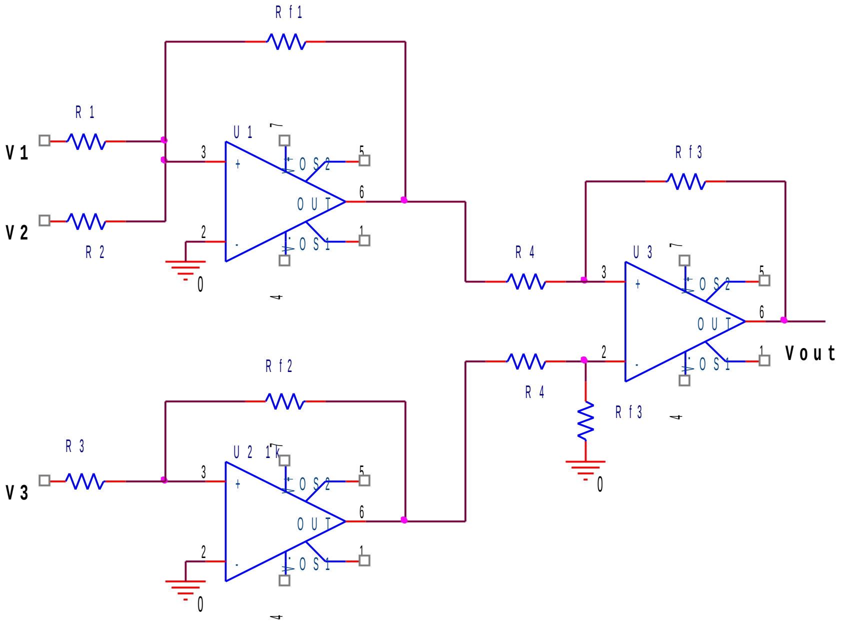


Y=X.A

There are only two states. So that number of flip-flops required = 1



Q.5) a) Design the op-amp circuit which can give the output as V_0=2*V1+4*V2-V3.



From circuit diagram:-

$$V = \frac{Rf3}{R4} \times (VB - VA)$$

Where as $V_B = -\frac{Rf2}{R3} \times V3$

$V_A = -\frac{Rf1}{R1} \times V1 - \frac{Rf1}{R2} \times V2$

Assume Rf3=Rf4=10KΩ

.’. $V = \frac{Rf1}{R1} \times V1 + \frac{Rf1}{R2} \times V2 - \frac{Rf2}{R3} \times V3$

But we want

$V_0 = 2*V1 + 4*V2 - V3$.

Comparing above equations with required equation

$\frac{Rf1}{R1} = 2$, $\frac{Rf1}{R2} = 4$, and $\frac{Rf2}{R3} = 1$

Assume Rf1=Rf2=10KΩ

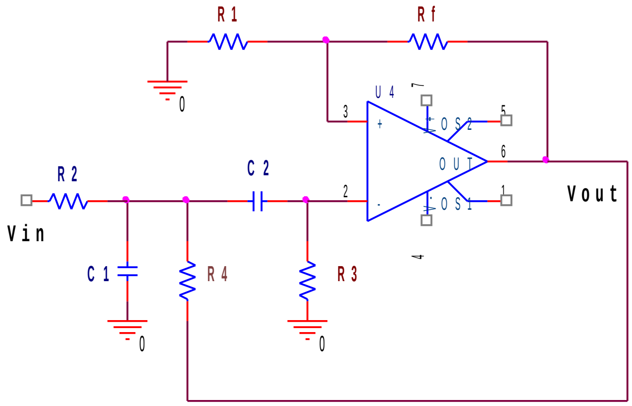
.’. R1=5 KΩ

R2=2.5KΩ

R3=10KΩ

Rf1=Rf2=Rf3=R4=10KΩ

Q.5) b) Design second order band pass filter (KRC) with f0=10 KHz and bandwidth=1 KHz, What is resonant gain?



Take C1=C2=C

We know that

$$w0=\frac{\sqrt{2}}{R\cdot C}$$

$$f0=\frac{\sqrt{2}}{2\cdot\Pi\cdot R\cdot C}$$

$$R=\frac{\sqrt{2}}{2\cdot\Pi\cdot f0\cdot C}$$

Assume C=0.01uF

.'. **R=2.250KΩ**

Calculate Q and K

$$Q=\frac{f0}{B.W}=\frac{10K}{1K}=10$$

$$K=4-\frac{\sqrt{2}}{Q}=4-\frac{\sqrt{2}}{10}=3.858$$

But we know that

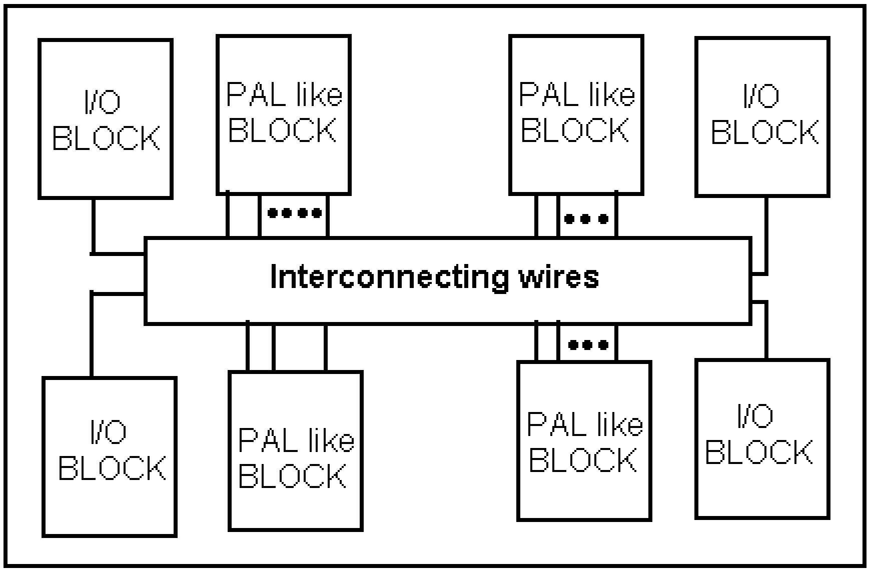
$$K=1+\frac{Rf}{R1}$$

Assume Rf=4.7KΩ

R1=1.644KΩ

Resonant gain=$H_{oBP}=\frac{K}{4-K}=27.16$

C) Draw and explain the block diagram of CPLD.

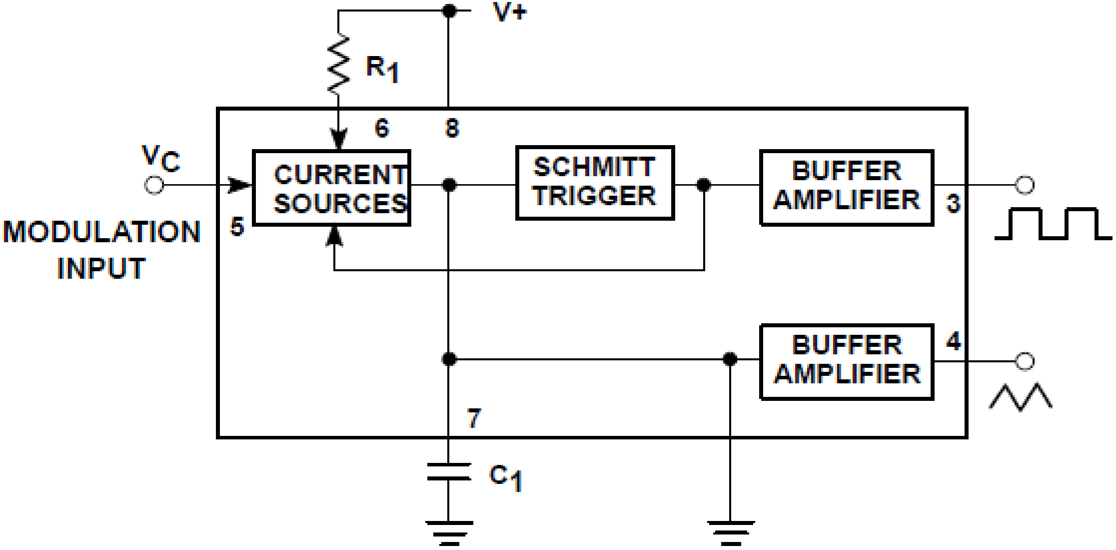


CPLD are capable of implementing logic circuit of up to 10000 equivalent gates.
It contains following blocks

- PAL like block
- I/O block
- Interconnecting wires

PAL like block contains 16 microcells. Each microcell consists of an AND-OR combination followed by EX-OR gates, flip-flop, multiplexers and tri-state buffer.
Every AND-OR combination contains about 5 to 20 AND gates and one OR gate. So OR gate has 5 to 20 inputs.
OR gate output is connected to the input of EX-OR gate. The EX-OR gate is used to invert the OR gate output.
The EX-OR gate output is stored into a D-FF.
Tri-state buffer acts as a switch. Corresponding pin of chip acts as output if the buffer is enabled and same pin acts as input pin if buffer is disable.

Explain VCO IC-566 and its features.



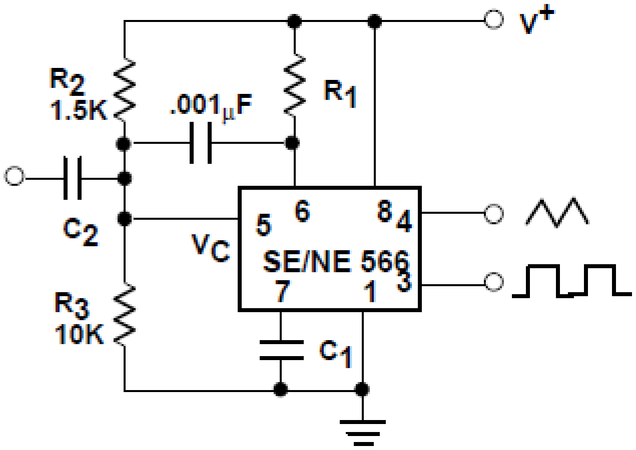
FEATURES

1) Wide range of operating voltage (up to 24V; single or dual)

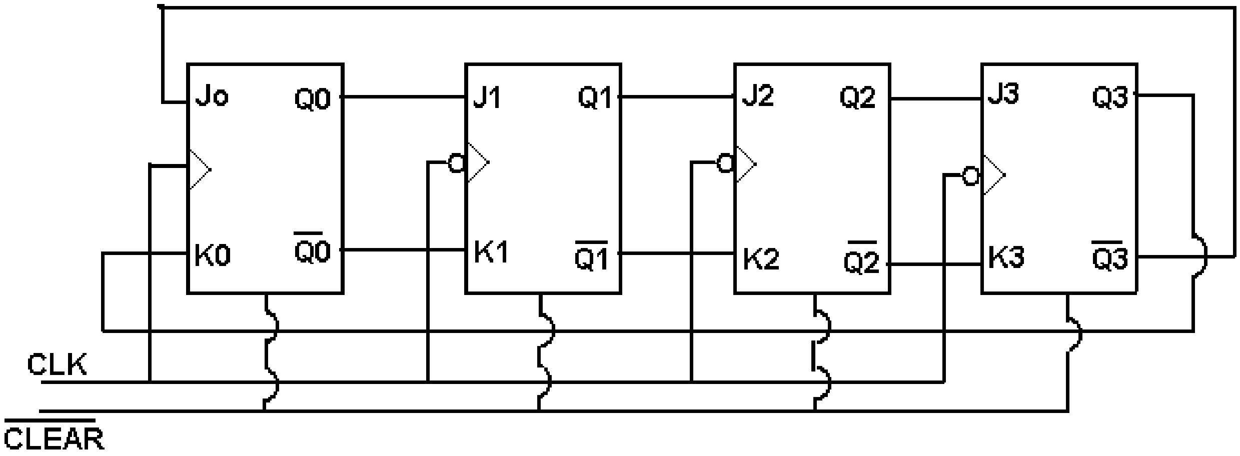
2) High linearity of modulation
3) Highly stable center frequency (200ppm/°C typical)
4) Highly linear triangle wave output
5) Frequency programming by means of a resistor or capacitor, voltage or current
6) Frequency adjustable over 10-to-1 range with same capacitor

In most cases, the frequency of an oscillator is determined by the time constant RC. However, in cases or applications such as FM, tone generators, and frequency-shift keying (FSK), the frequency is to be controlled by means of an input voltage, called the control voltage. This can be achieved in a voltage-controlled oscillator (VCO). ***A VCO is a circuit that provides an oscillating output signal (typically of square-wave or triangular waveform) whose frequency can be adjusted over a range by a dc voltage***. An example of a VCO is the 566 IC unit, that provides simultaneously the square-wave and triangular-wave outputs as a function of input voltage. The frequency of oscillation is set by an external resistor R_1 and a capacitor C_1 and the voltage V_c applied to the control terminals. Figure shows that the 566 IC unit contains current sources to charge and discharge an external capacitor C_v at a rate set by an external resistor R_1 and the modulating dc input voltage. A Schmitt trigger circuit is employed to switch the current sources between charging and discharging the capacitor, and the triangular voltage produced across the capacitor and square-wave from the Schmitt trigger are provided as outputs through buffer amplifiers. Both the output waveforms are buffered so that the output impedance of each is 50 f2. The typical magnitude of the triangular wave and the square wave are 2.4 $\mathbf{V_{peak\text{-}to\text{-}peak}}$ **and** $\mathbf{5.4V_{peak\text{-}to\text{-}peak}}$.

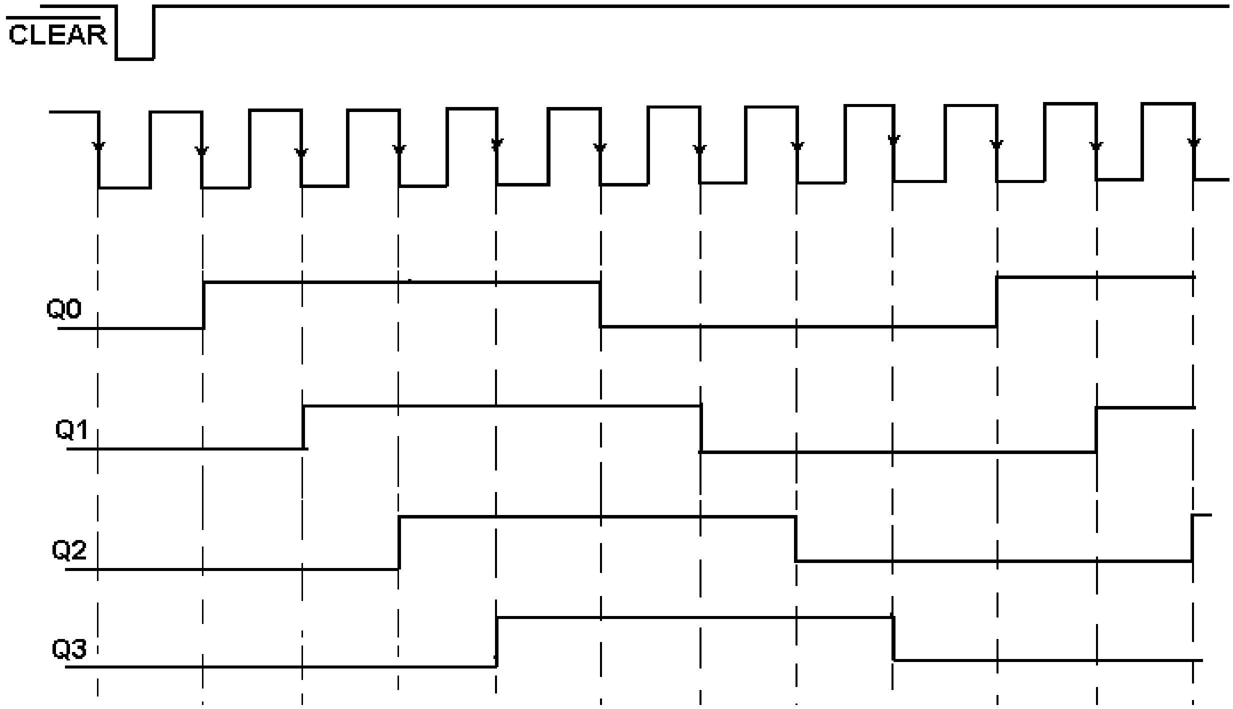
$$f_{out} = 2(V^+ - V_c)/R_1C_1V^+$$



B) Draw a logic diagram and timing diagram of 4-bit Johnson's counter.



CIRCUIT DIAGRAM

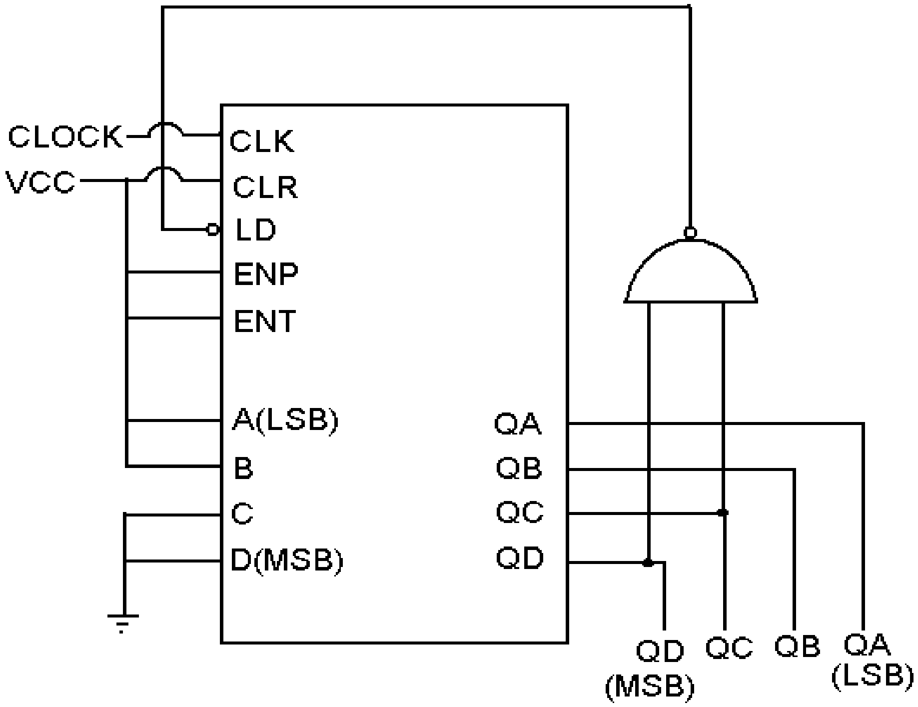


WAVEFORM FOR JOHNSON’S COUNTER

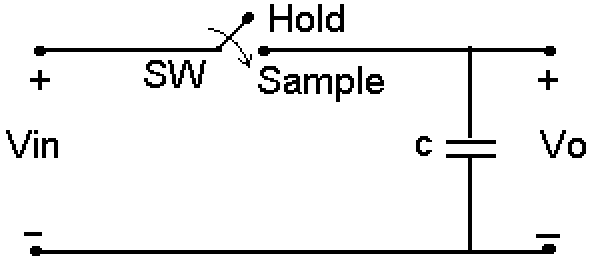
c) Give the features of function generator IC-566.

-- Low sine wave distortion, 0.5%, typically.
-- Wide sweep range, 2000:1, typically
-- Low supply sensitivity.
-- Adjustable duty cycle.
-- Linear amplitude modulation.

d) Design excess-3 decimal counter using MSI IC-74×163



Q.7) Explain the operation of basic sample and hold circuit.

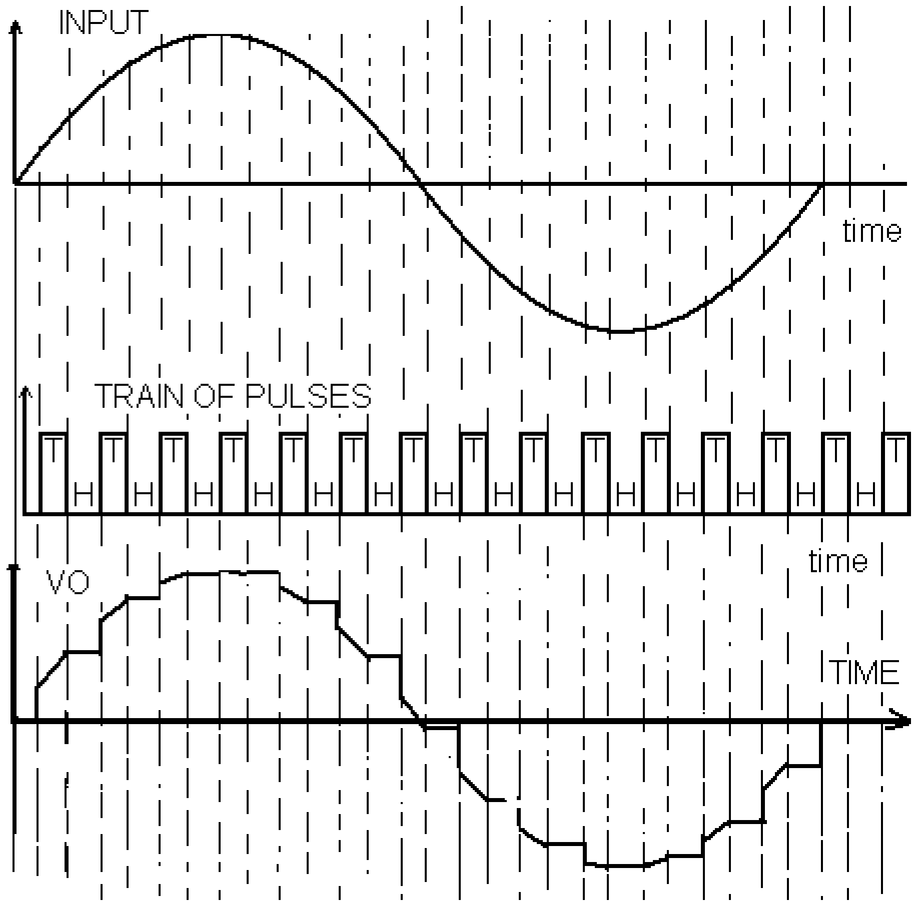


Basic sample and hold circuit has one input and one output. Electronic switch can be controlled by a control signal. There are two possible modes of operation namely sampling and hold mode, depending on the position of switch.

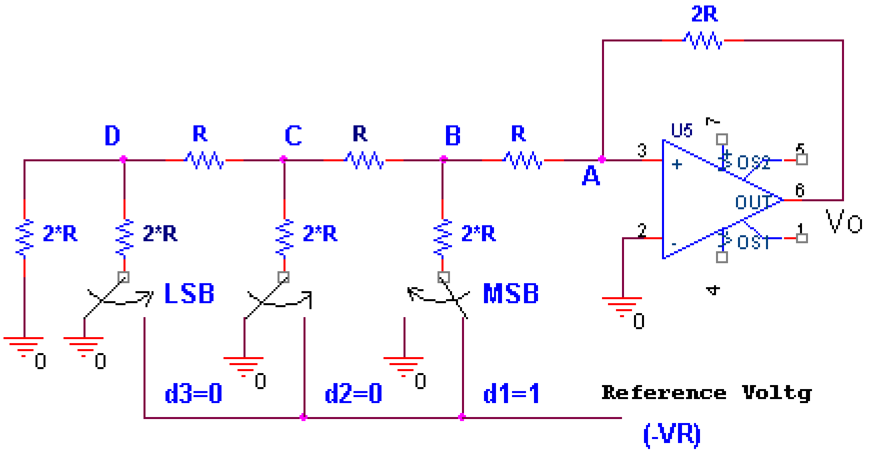
In sampling mode switch is in the close position, and capacitor charges to it's the instantaneous input voltage. This is called as sapling process.

In hold mode, switch position is open. The capacitor is now disconnected from input.

As there is no path for capacitor to discharge, it will hold voltage which was present on it just before opening the switch. Capacitor will hold this voltage till next sampling instant.



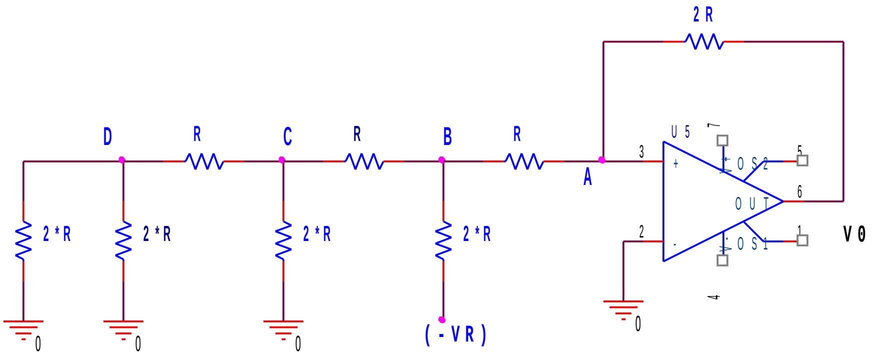
B) Draw the circuit diagram of 4-bit R-2R ladder converter and derive its output voltage.



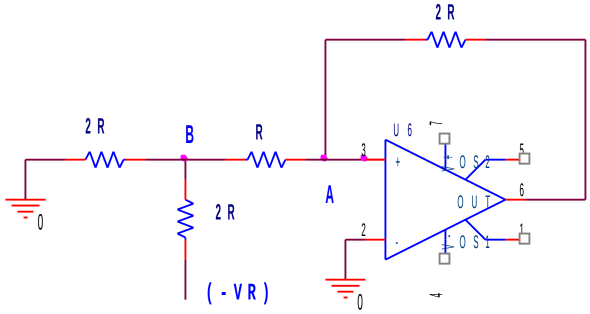
Operation of R-2R ladder DAC.

Number of digit per binary word is assume to be 3.(i.e. n=3). Switch position indicates that the binary word is $d_1.d_2.d_3$

Original circuit can be simplified as

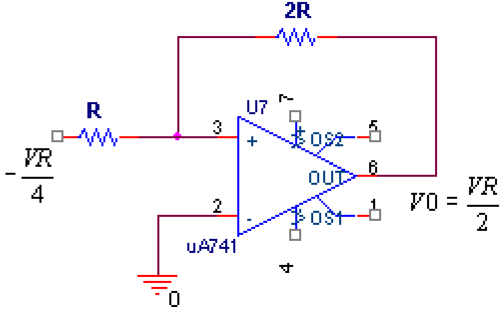


Applying Thevenin’s theorem at B



$$VB=\frac{(\frac{2\cdot R}{3})}{2\cdot R+\frac{2}{3}R}\cdot -VR \qquad \text{VB}=-\frac{VR}{4}$$

Considering op-amp to be an inverting amplifier the equivalent circuit of DAC is shown in figure.



For binary input $d_1.d_2.d_3$=100… Vo=$\frac{VR}{2}$.

Similarly we can derive op-amp output voltage for various input combinations.