

**SUBJECT: MICROPROCESSOR & MICROCONTROLLER I**

**PAPER SOLUTION 2009-2010**

**SUBMITTED BY MS.S.B.KAMBLE**

Q.NO.1;a)

i) ROM=4K byte=4k\*8 Using 4k\*4

no.of chips=4k\*8/4k\*4

EPROM=2 chips

RAM=8K byte=8k\*8 Using 2k\*4

no.of chips=8k\*8/2k\*8

EPROM=4chips

ii) Address lines:-

We can interface 4k byte ROM & 8k byte RAM using 4k\*4 & 2k\*8 devices respectively.

12 Address lines required for EPROM of 4k

11 Address lines required for RAM of 2K

To calculate the Address:-

We can use A0-A11 lines for address calculation.

S.A. of ROM (1)=0000 H

E.A.of ROM (1)=0FFF H

S.A. of ROM (2)=1000 H

E.A.of ROM (2)=1FFF H

S.A. of RAM (1)=2000 H

E.A.of RAM (1)=2FFF H

S.A. of RAM (2)=3000 H

E.A.of RAM (2)=3FFF H

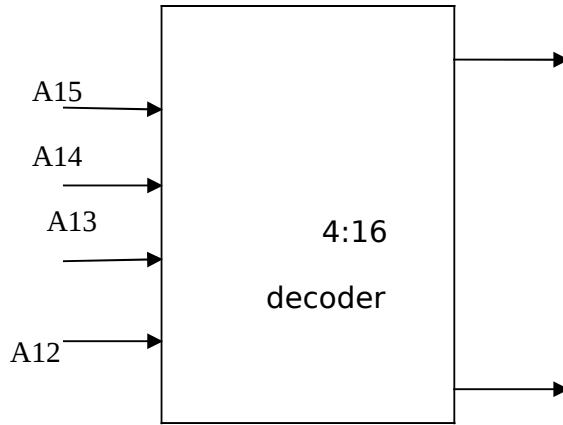
S.A. of RAM (3)=4000 H

E.A.of RAM (3)=4FFF H

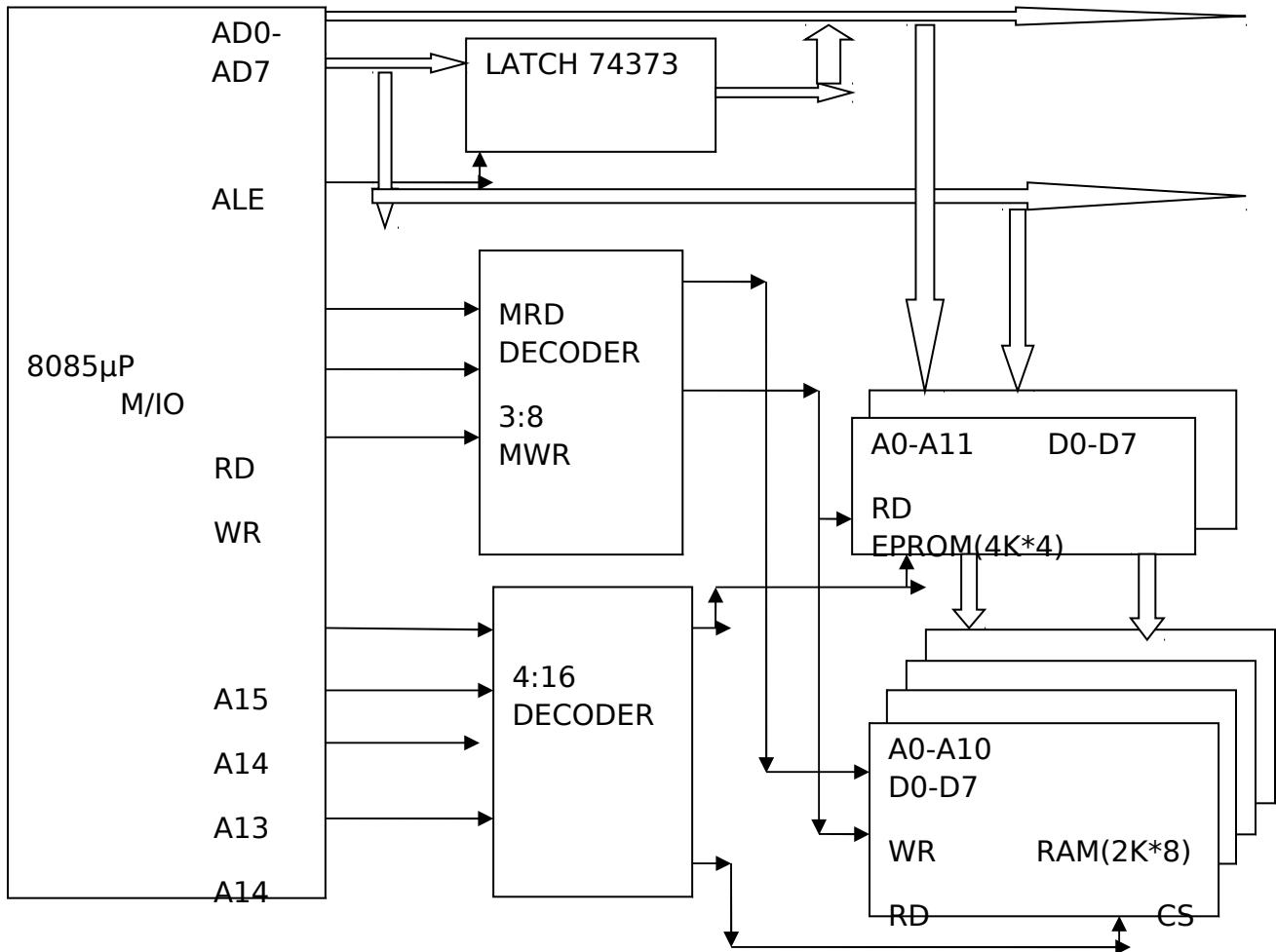
S.A. of RAM (4)=5000 H

E.A.of RAM (4)=5FFF H

iii) Decoder logic.



iv) Final implementation:-



Q.No.1) b) program:

Start:-MVI C, 05 H

LXI H,2000 H

LXI D,3000 H

UP: MOV A,M

ANI OFO H

RRC

RRC

RRC

RRC

STAX,D

INX D

MOV A,M

ANI OF H

STAX,D

INX H

DCR C

JNZ U P

Q.No.2) a)

:-

8085 supports two types of interrupts.

i) H/W interrupt:-

Peripheral device activates interrupt by activating the respective pin.

These types of interrupt, where up pins are used to receive interrupt request are called H/W interrupts.

The  $\mu p$  has five H/W interrupts they are:-

- i) TRAP
- ii) RST 1.5
- iii) RST 6.5
- iv) RST 5.5
- v) INTR

ii) Software interrupts:-

In case of S/W interrupts the cause of the interrupt is the execution of instruction.

The  $\mu p$  has eight instructions.

These eight instructions are RST0 to RST7

- a) TRAP :- It is non maskable ,edge level triggered interrupt.it has highest priority among all interrupt.it is used for emergency purpose.
- b) RST 7.5: -It is maskable ,edge level triggered interrupt.it has highest priority among all maskable interrupt & 2<sup>nd</sup> priority among all interrupt.
- c) RST 6.5 & RST 5.5:- It is maskable ,level triggered interrupts.Using SIM instruction they can be set or reset
- d) INTR:- It is maskable ,level triggered interrupts.

Q.NO.2) b)

i) square wave freq. =1 KHZ.

Time period = 1/freq. = 1/1KHZ = 1 MSEC.

Time period = TON + TOFF.

TON + TOFF = 0.5 msec.

ii) LXI SP,FFFF H

MVI A,40 H

Up:SIM

CALL DELAY

MVIA,CO H

SIM

CALL DELAY-Delay of 0.5 ms.

JMP UP.

iii) Delay calculation:-

Assume that counter 0 is used.

Here address, B 0=Counter 0

B 1=Counter 1

B2=Counter 2

& B3=Control register

To generate square wave of 1 KHZ with 30 HZ Clk freq.

Clk freq/freq.

30 KHZ/1 KHZ=(30)d=(1E)H

Control word:-

0	0	0	1	0	1	1	1
Counter 0	load LSB only		square wave generator		BGD or o-Binary.		

MVI A,17 H

OUT B3 H

MVI A,1E H

OUT B 0 H.

OR,

DELAY:MVI A, IEH

DCR A

JNZ DELAY.

Q.NO.3)a)

The 8155 having two handshake modes.

- i) Interrupt i/p with handshake signal.
- ii) Interrupt o/p with handshake signal.

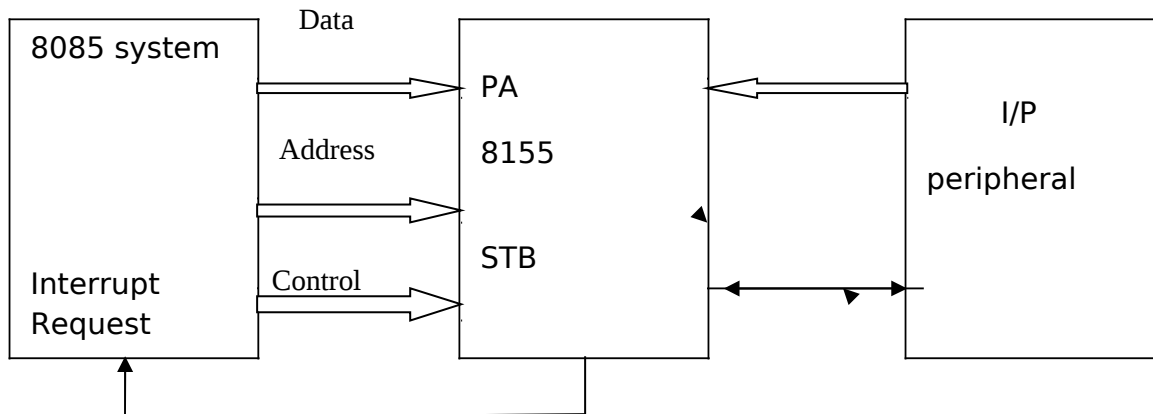
The functions of ports are defined with logic 1-o/p & logic 0-i/p by writing command word.

In Handshake mode the data transfer takes place between  $\mu$ p system & peripheral using control signals called as handshake signals.

Port A & port B can be configured in handshake mode as i/p /o/p each uses port c bits as handshake signals ALT 3 allows PORT A in handshake mode.

ALT 4 allows both PORT A & PORT B in handshake mode.

Handshaking signals:-



a] STB strobe i/p:-

It is active low i/p signal to 8155,activated by peripheral for data transfer.

When peripheral is ready for data transfer from or to 8155,it activates STB & send or received data

b] BF Buffer full:-

It is active high o/p signal generated by 8155to indicate availability of data in port.

When data is transferred from 8155 to peripheral,the BF signal used to signal peripheral to read it.

When data is transferred from peripheral to 8155,BF indicate the data is still not sent to 8085 so don't send next data byte.

c] INTR:-Interrupt request.

Interrupt the CPU 8085.

d] IE :-Interrupt enable:-

Explanation:-

When peripheral device contains data to be transferred to 8085 through 8155,it places data into the i/p port along with STB low to indicate the data is transferred to 8155.

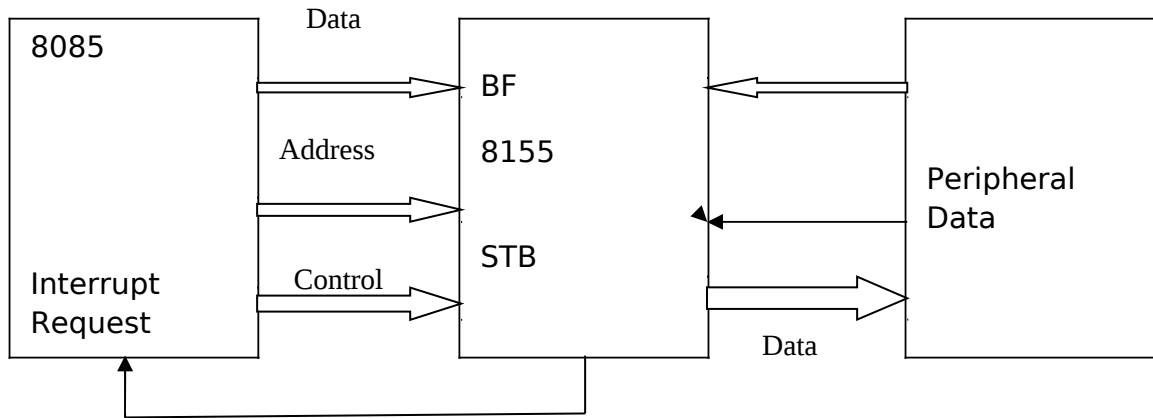
BF is used by peripheral for next data transfer during the falling edge of STB.

On the rising edge of STB the data gets latched into PORT & INTR is generated by internal bit is set in command register.

The INTR is connected to interrupt request of 8085, gets interrupt & branches to ISR.In ISR a program to read data from 8155 port is written so the 8085 generate the RD signal to read data from 8155 port.

After 8085 completes the data read option the signals BF & INTR will be removed.

b) Handshake o/p mode:-



If o/p port is empty, 8085 writes data to 8155 port. The checking of port can be done by using interrupt signal or status read option.

The write option is performed by using wr signal.

The falling edge of WR signal resets INTR if INTR is generated & rising edge sets BF.

The BF set informs peripheral that the data is available in port.

Because of BF signal the peripheral reads data from 8155 & ack by STB signal.

The STB signal resets BF signal & generates interrupt request INTR to the processor to indicate the previous data byte is read by peripheral & next data byte should be written in o/p port.

Q.NO.3)b)Program:-

MVI A, 80 H

OUT CWR.

Main: MVI B, 08 H

MVI C,7 FH

LXI H, MSG.

UP: MOV A,C

OUT P B

MOV A,M

OUT P A

CALL DELAY.

MOV A,C

RRC

MOV C,A

INX H

DCR B

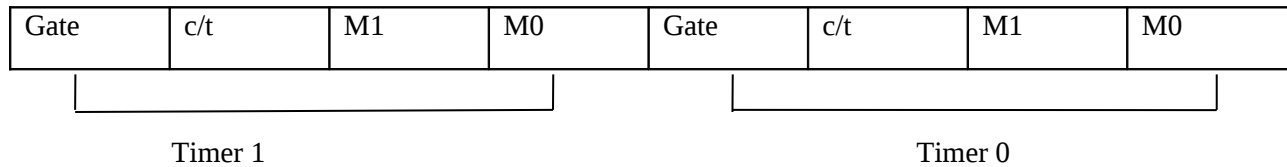
JNZ UP

RET

MSG: DW "WEL-DONE".

Q.NO.4)A)

I) TMOD Register



M1	M0	
0	0	8 bit Timer/counter THX with TLX as 5-bit prescalar
0	1	16-bit timer/counter THX & TLX are cascaded,
1	0	8-bit auto reload timer/counter THX holds a value which is to be reloaded into TLX.
1	1	TLO is an 8-bit control by timer 0 control bits.
1	1	timer/counter 1 stopped.

II) TCON TIMER/Counter control register:-

TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0
-----	-----	-----	-----	-----	-----	-----	-----

TF1- Timer 1 overflow flag.

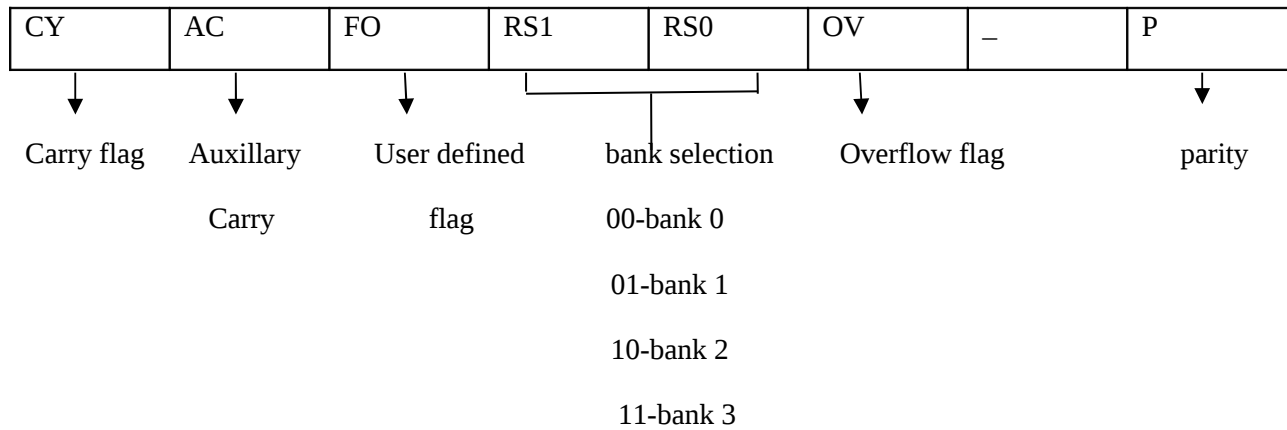
TR1- Timer 1 Run control bit.

IE1- Interrupt 1 Edge flag.

IT1- Interrupt 1 type control bit.

Q.NO.4)B)

Program status word.



i) Carry flag :- When there will be a carry or borrow out of MSB (D7)bit of result.

e.g. ADD A,#-80 H

A=10100001 H.

10100001

+ 10000000

---

00100001

7 Carry.

ii) Axillary carry:-

Whenever there is a carry out of the lower nibble into higher nibble.

e.g A=00001010

+ 10001000

---

10010010

Ac

iii)Overflow flag:-

if an arithmetic overflow has occurred.

e.g MOV A, # 12 H

MOV B, # 10 H

MUL A,B.

After option, result is greater than 8-bit.

Overflow flag will be set.

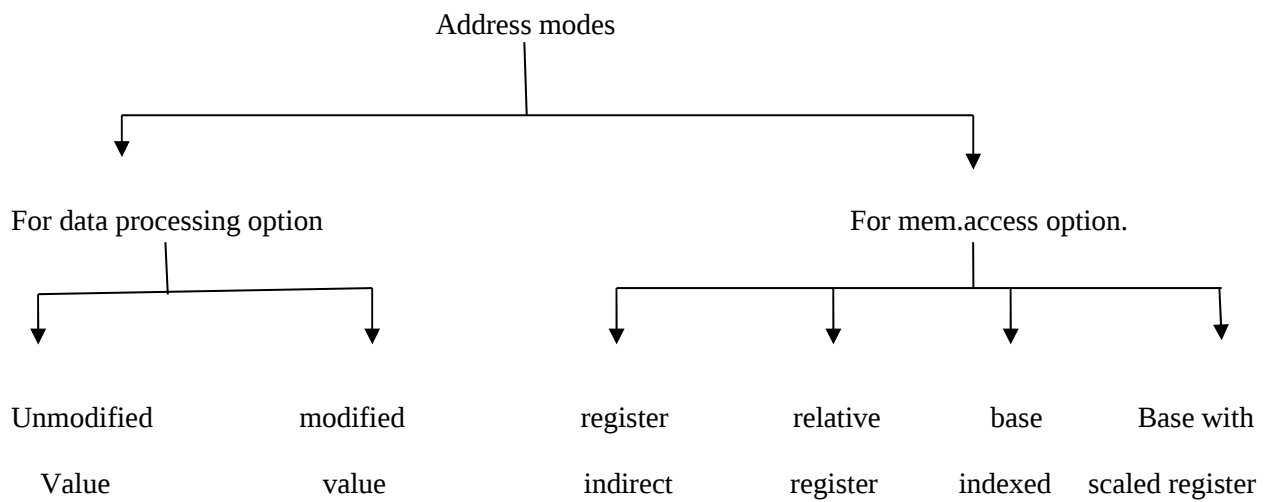
iv) Parity flag:-

When result has even parity i.e. even number as is.

Even parity flag will be set.

v) The 8051 has three general purpose user flag that can be set to 1 or cleared to 0 by programmer.

Q.no.5)a):-



For data processing option:-

1) Unmodified value:-

`MOV R0,# 1234 H`

The register or a value is given modified.

2) Modified value:-

Logical shift left.

`MOV R0,R1,LSL # 2.`

Address modes for memory access operands.

i) Register indirect address mode:-

`LDR R0,[R1].`

ii) Relative register indirect address mode:-

LDR RO,[R1,#4].

iii) Base indexed indirect address mode:-

LDR RO,[R1,R2]

iv) Base with scaled register address mode:-

LDR RO,[R1,R2,LSL#2]

Q.NO.5)b)

i) BCC up:- This instruction will branch to label if carry flag is clear.

ii) RSB RD,RS1,RS2.

$RD \leftarrow RS2 - RS1$

iii) MLA R4,R3,R2,R6.

$R4 \leftarrow R3 * (R2 + R6)$

iv)

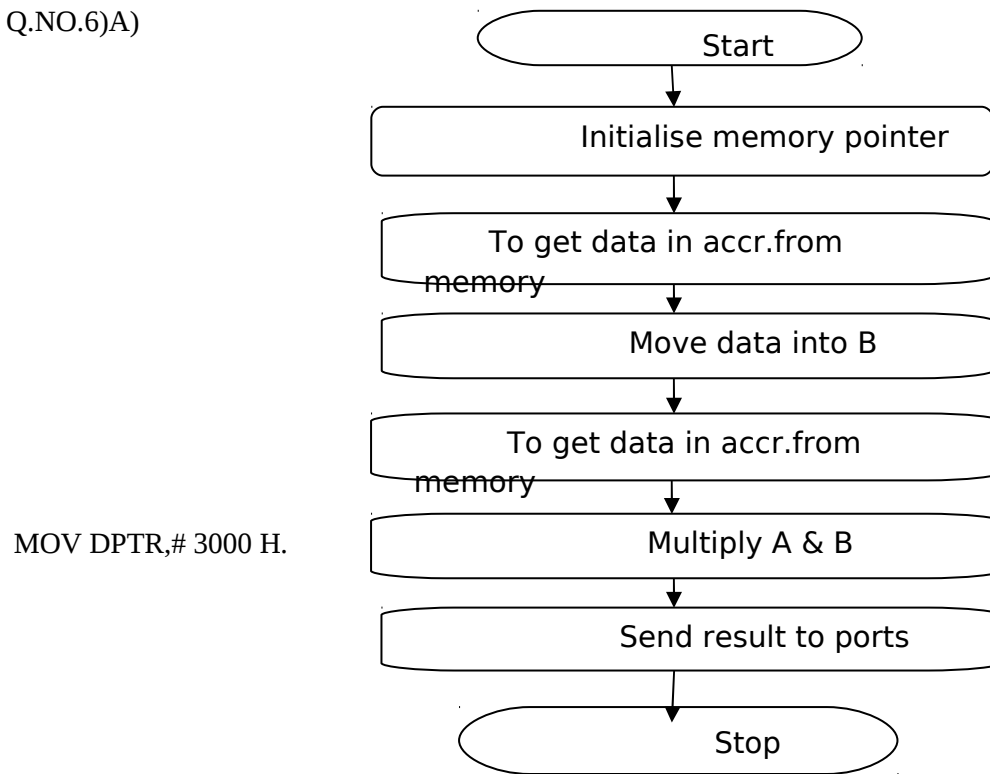
SWP R1,R2,[R3]

This instruction will load register r1 with the word addressed by register r3 & store register r2 at r3.

v) CDP P4,3,C12,C13,C3,4.

It is coprocessor 4 data option such that opcode-1=3,opcode-2=4,destination register is c12 & source register are c13 & c3.

Q.NO.6)A)



MOV X A,@ DPTR.

MOV B,A.

INC DPTR.

MOVX A, @ DPTR

MUL AB.

MOV P1,A

MOV P3,B.

OR,AOnly program:-

Q.NO.6)b):-

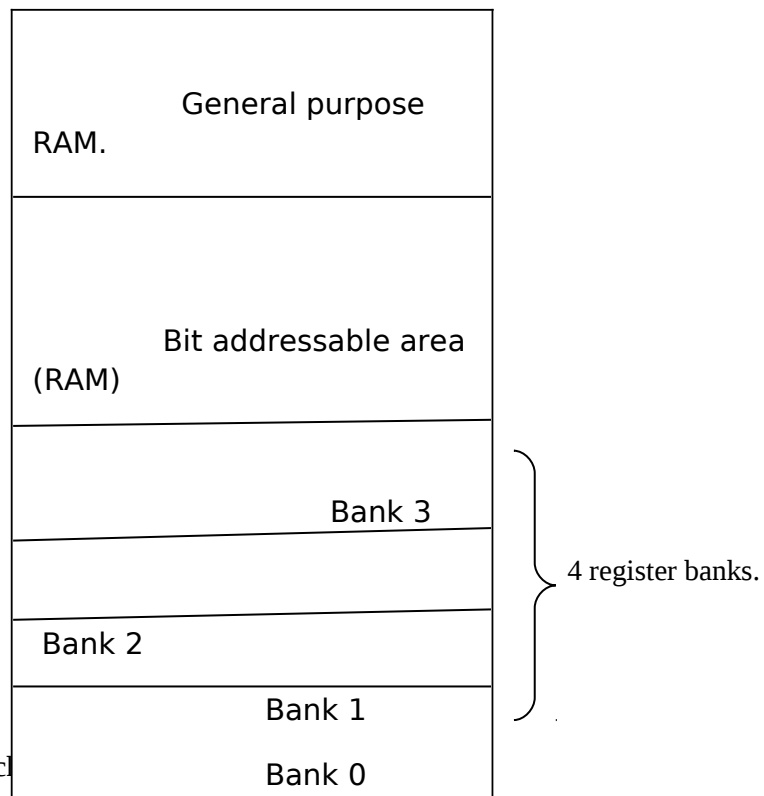
The 8051 has an internal RAM & ROM.

Internal RAM:- This is organized in three parts.

1] Four register banks of 8 bytes each.

2] Bit addressable area of 16 bytes.

3] General purpose.RAM.



1] Four register banks of 8 bytes each

Each bank is made up of eight registers named Ro to Ry.

Intotal 32 bytes working register from 00 to 1f.

For bank selection two bits are used from PSW i.e. RS0 & RS1.

2] Bit addressable area of 16 bytes:-

Range 20 H to 2FH.

16 bytes provide us with 128 bites forming addressable bits.

3] General purpose RAM area:-

Scarch pad area.

Range-30 H to 7 F H.

Q.NO.7)A)

Device	EPROM	RAM	Freq.MHZ	I/O Pins	UART	16-BIT Timer	Interrupt
89c51	4	128	24	32	1	2	6
89c52	8	256	24	32	1	3	8
89c2051	1	64	24	15	1	1	6
89c2052	2	128	24	15	1	2	6

Atleast 6 points.

Q.NO.7)B)

There are two possible step modes.

Mode 1:- full stepping l.

In this case the motor mover by one step to do this 2 bits are changed at a time bit pattern are as follows:-

Step	A	B	C	D
1	1	0	0	1

2	1	0	1	0
3	0	1	1	0
4	0	1	0	1

Mode 2 :-Half stepping:-

In this case,the motor moves by some degrees. To do this 1 bit is changed at a time.

Q.7)c) Memory access instruction:

LDR R0,[R1]

LDR R0,[R1,#4]

LDR R0,[R1,#4]!

LDR R0,[R1,R2]

LDR R0,[R1,R2]!

LDR R0,[R1,R2,LSL#2]

Branching instruction:

BCC LABEL

BNE LABEL

BL FUNCTION

BLX LABEL

BX FUNCTION

